

TC74HC563AP/AF TC74HC573AP/AF/AFW

Octal D-Type Latch with 3-State Output

TC74HC563A Inverted

TC74HC573A Non-Inverting

The TC74HC563A and TC74HC573A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and output enable input (\overline{OE}).

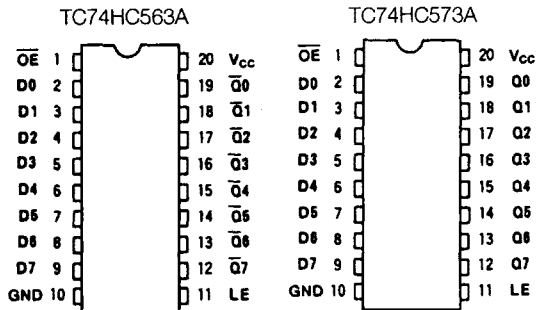
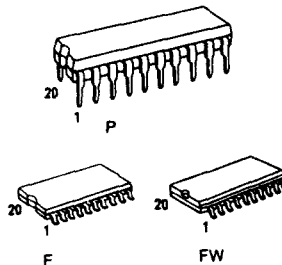
When the \overline{OE} input is high, the eight outputs are in a high impedance state.

The TC74HC563A has inverting outputs, and TC74HC573A has non-inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High Speed: $t_{pd} = 13ns$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min)
- Output Drive Capability: 15 LSTTL Loads
- Symmetrical Output Impedance: $I_{OH} = I_{OL} = 4mA$ (Min.)
- Balanced Propagation Delays: $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range: $V_{CC}(opr) = 2V \sim 6V$
- Pin and Function Compatible with 74LS563/573



Pin Assignment

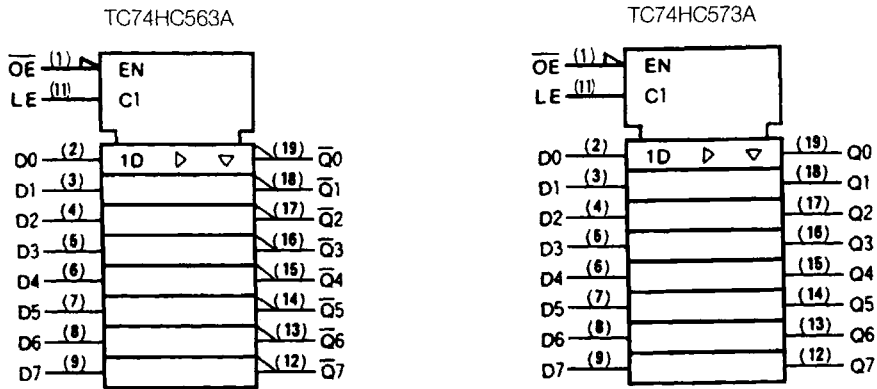
Truth Table

Inputs			Outputs	
\overline{OE}	LE	D	Q(HC573A)	\overline{Q} (HC563A)
H	X	X	Z	Z
L	L	X	Q_n	\overline{Q}_n
L	H	L	L	H
L	H	H	H	L

X: Don't Care

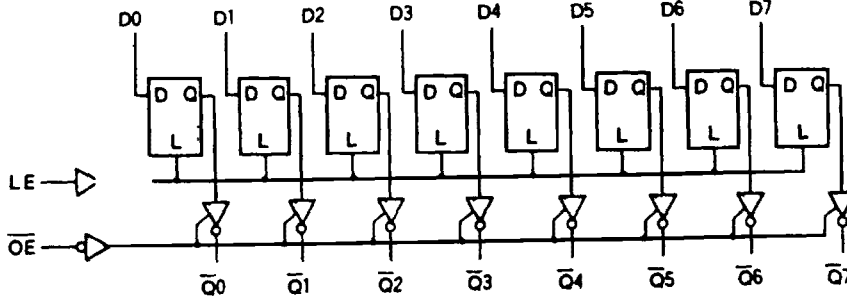
Z: High Impedance

Q_n (\overline{Q}_n): Q(\overline{Q}) outputs are latched at the time when the input is taken to a low logic level.

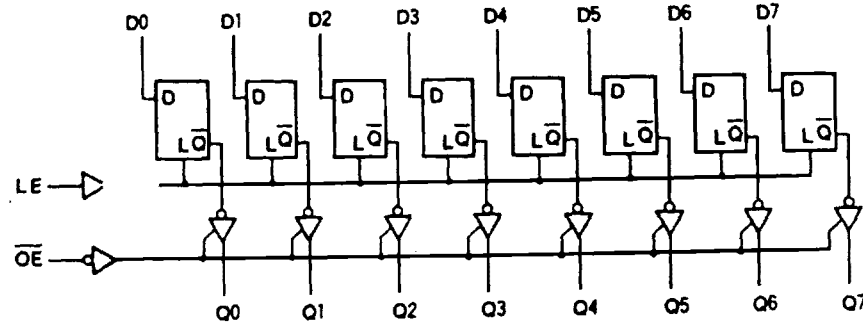


IEC Logic Symbol

TC74HC563A



TC74HC573A



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC} /Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*7180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0-1000($V_{CC} = 2.0\text{V}$) 0 - 500($V_{CC} = 4.5\text{V}$) 0 - 400($V_{CC} = 6.0\text{V}$)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition	$T_a = 25^{\circ}\text{C}$				$T_a = -40 \sim 85^{\circ}\text{C}$		Unit	
			V_{CC}	Min.	Typ.	Max.	Min.	Max.		
High-Level Input Voltage	V_{IH}	-	2.0	1.5	-	-	1.5	-	V	
			4.5	3.15	-	-	3.15	-		
			6.0	4.2	-	-	4.2	-		
Low-Level Input Voltage	V_{IL}	-	2.0	-	-	0.5	-	0.5	V	
			4.5	-	-	1.35	-	1.35		
			6.0	-	-	1.8	-	1.8		
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
				4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
				4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	-	-	±0.5	-	±5.0	μA	
			6.0	-	-	±0.1	-	±1.0		
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	±0.1	-	±1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	4.0	-	40.0		

Timing Requirements (Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C		Ta = -40 ~ 85°C		Unit
			V _{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (LE)	$t_{W(H)}$ $t_{W(L)}$	-	2.0	-	75	95	ns
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Setup Time (Data)	t_s	-	2.0	-	50	65	
			4.5	-	10	13	
			6.0	-	9	11	
Minimum Removal Time (Data)	t_h	-	2.0	-	5	5	
			4.5	-	5	5	
			6.0	-	5	5	

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit	
			CL	V _{CC}	Min.	Typ.	Max.		Min.
Output Transition Time	t_{TLH} t_{THL}	-	50	2.0	-	20	60	-	75
				4.5	-	6	12	-	15
				6.0	-	5	10	-	13
Propagation Delay Time (LE-Q, \bar{Q})	t_{PLH}	-	50	2.0	-	50	115	-	145
				4.5	-	15	23	-	29
				6.0	-	13	20	-	25
	t_{PHL}		150	2.0	-	60	155	-	195
				4.5	-	20	31	-	39
				6.0	-	17	26	-	33
Propagation Delay Time (D-Q, \bar{Q})	t_{PLH}	-	50	2.0	-	42	110	-	140
				4.5	-	14	22	-	28
				6.0	-	12	19	-	24
	t_{PHL}		150	2.0	-	57	150	-	190
				4.5	-	19	30	-	38
				6.0	-	16	26	-	32
Output Enable Time	t_{OZL}	$R_L = 1\text{k}\Omega$	50	2.0	-	55	140	-	175
				4.5	-	17	28	-	35
				6.0	-	14	24	-	30
	t_{OZH}		150	2.0	-	66	180	-	225
				4.5	-	22	36	-	45
				6.0	-	19	31	-	38
Output Disable Time	t_{OLZ} t_{PHZ}	$R_L = 1\text{k}\Omega$	50	2.0	-	40	125	-	155
				4.5	-	17	25	-	31
				6.0	-	15	21	-	26
Input Capacitance	C _{IN}		-	-	-	5	10	-	10
Output Capacitance	C _{OUT}		-	-	-	10	-	-	-
Power Dissipation Capacitance	C _{PD(1)}		TC74HC563A	-	-	49	-	-	-
		TC74HC573A	-	-	51	-	-	-	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(OP)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 33 + 16 \cdot n \text{ (TC74HC563A)}$$

$$C_{PD}(\text{total}) = 33 + 18 \cdot n \text{ (TC74HC573A)}$$