

# SN54ABT16952, SN74ABT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS082A – D3801, FEBRUARY 1991 – REVISED OCTOBER 1992

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-IIIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

## description

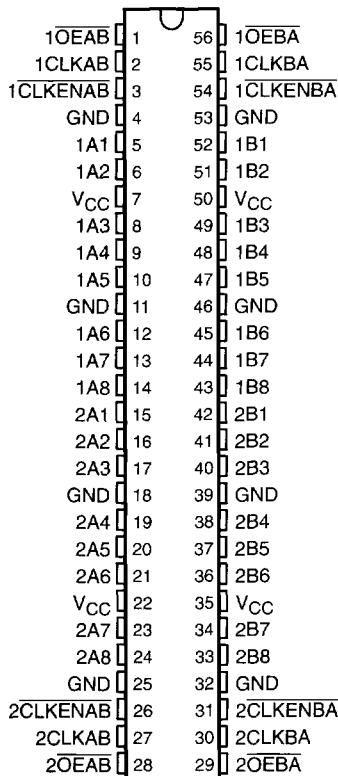
The 'ABT16952 is a 16-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16952 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ( $\overline{\text{CLKENAB}}$  or  $\overline{\text{CLKENBA}}$ ) input is low. Taking the output-enable ( $\overline{\text{OEAB}}$  or  $\overline{\text{OEBA}}$ ) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16952 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16952 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16952 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT16952 . . . WD PACKAGE  
SN74ABT16952 . . . DGG OR DL PACKAGE  
(TOP VIEW)



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**FUNCTION TABLE†**

INPUTS				OUTPUT B
CLKENAB	CLKAB	OEAB	A	
H	X	L	X	B <sub>0</sub> ‡
X	L	L	X	B <sub>0</sub> ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

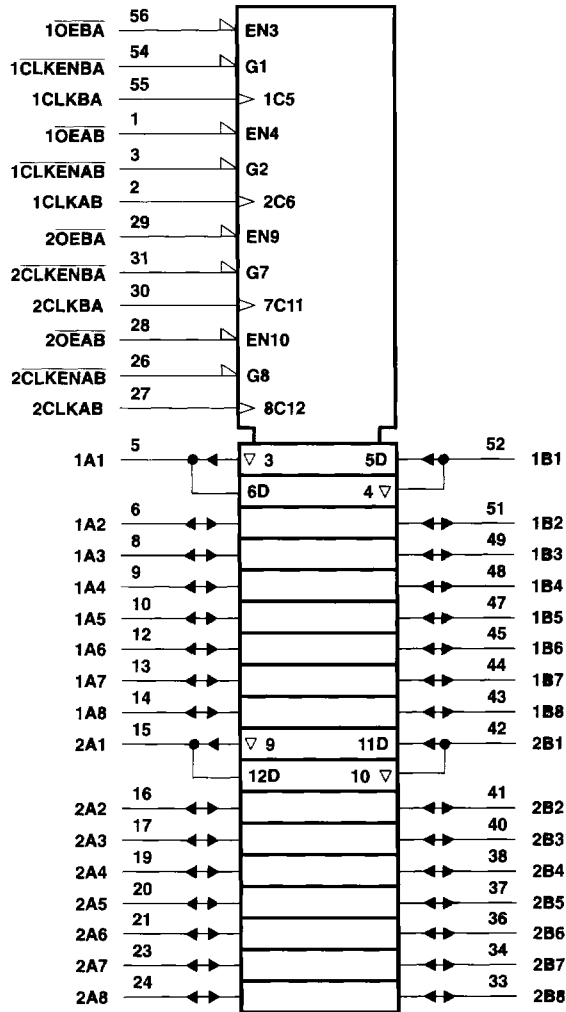
† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENB $\bar{A}$ , CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

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logic symbol†

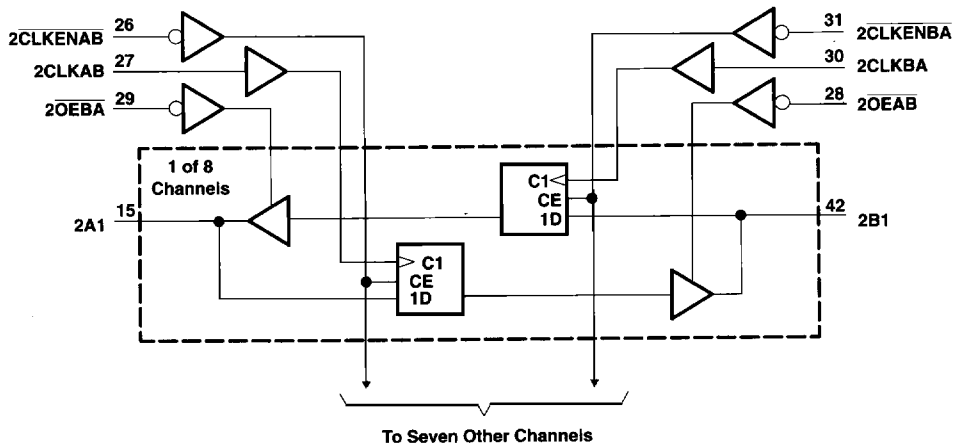
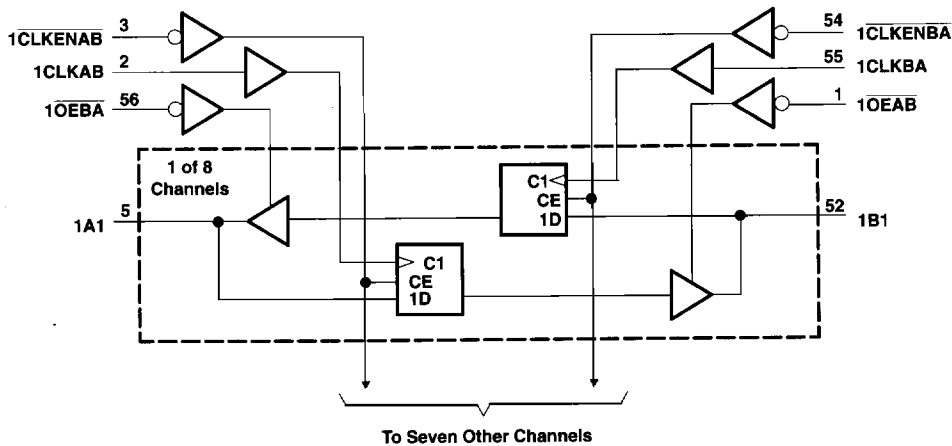


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16952 .....	96 mA
SN74ABT16952 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package .....	1 W
DL package .....	1 W
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## recommended operating conditions (see Note 2)

		SN54ABT16952		SN74ABT16952		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16952		SN74ABT16952		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2				-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5			2.5	V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3			3		
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2			2					
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA	2‡						2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA			0.55		0.55			V	
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA			0.55‡				0.55		
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	Control inputs		±1		±1		±1	μA	
		A or B ports		±100		±100		±100		
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50		50		50	μA	
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50		-50		-50	μA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high		50		50		50	μA	
I <sub>O</sub> ¶	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V			-50 -100 -200		-50 -200		-50 -200	mA	
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	A or B ports	Outputs high		2		2		2	mA
			Outputs low		35		35		35	
			Outputs disabled		2		2		2	
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			0.5		0.5		0.5	mA	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V	Control inputs		3					pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	A or B ports		8.5					pF	

† All typical values are at V<sub>CC</sub> = 5 V.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16952		SN74ABT16952		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	0	150	0	150	MHz
t <sub>w</sub> <sup>†</sup>	Pulse duration, CLKAB or CLKBA high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, before CLKAB <sup>†</sup> or CLKBA <sup>†</sup>	A or B	3.5	3.5		3.5		ns
		CLKENAB or CLKENBA	3	3		3		
t <sub>h</sub>	Hold time, after CLKAB <sup>†</sup> or CLKBA <sup>†</sup>	A or B	1	1		1		ns
		CLKENAB or CLKENBA	1	1		1		

<sup>†</sup> This parameter is specified by design but not tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

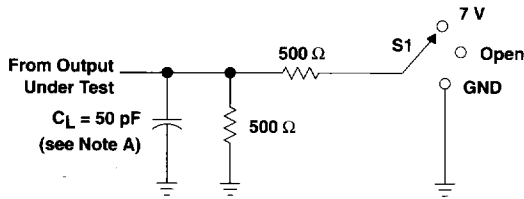
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16952		SN74ABT16952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150		150		MHz
t <sub>PLH</sub>	CLK	A or B	1	2.6	3.9	1	4.4	1	4.3	ns
t <sub>PHL</sub>			1	2.6	4.2	1	4.6	1	4.5	
t <sub>PZH</sub>	OE	A or B	1	2.5	3.8	1	4.7	1	4.6	ns
t <sub>PZL</sub>			1	2.8	5.1	1	6.1	1	6	
t <sub>PHZ</sub>	OE	A or B	1.7	3.4	4.7	1.7	6.1	1.7	5.5	ns
t <sub>PLZ</sub>			1.3	3	3.9	1.3	4.8	1.3	4.2	

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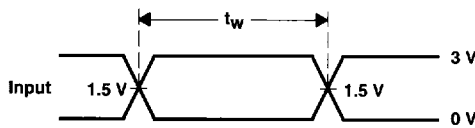
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PARAMETER MEASUREMENT INFORMATION

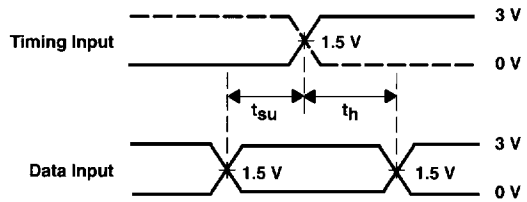


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

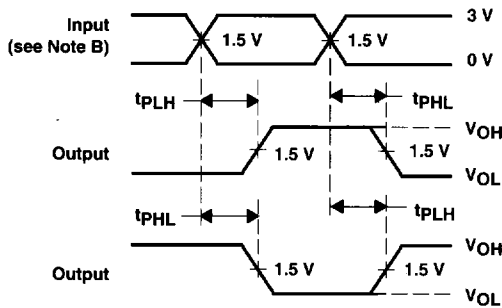
LOAD CIRCUIT FOR OUTPUTS



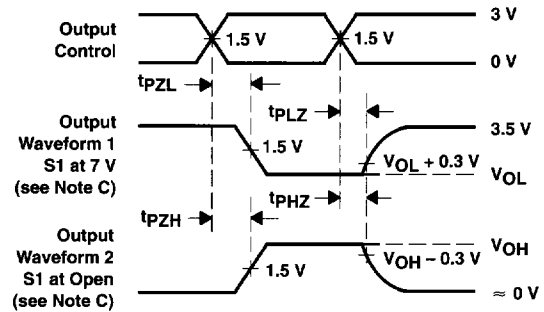
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

