



UC3842B/3843B

LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

DESCRIPTION

The UTC **UC3842B/3843B** are specifically designed for off-line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components.

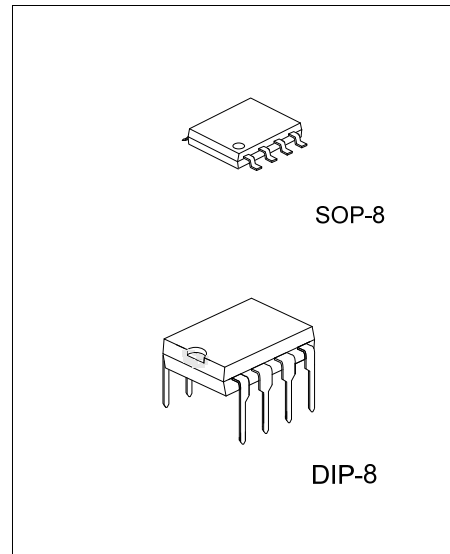
The **UC3842B** has UVLO thresholds 16V (on) and 10V(off), ideally suited for off-line converters. The **UC3843B** is tailored for lower voltage applications having UVLO thresholds of 8.4V(on) and 7.6V(off).

FEATURES

- * Trimmed oscillator for precise frequency control
- * Oscillator frequency guaranteed at 250kHz
- * Current mode operation to 500kHz
- * Automatic feed forward compensation
- * Latching PWM for cycle-by-cycle current limiting
- * Internally trimmed reference with undervoltage lockout
- * High current totem pole output
- * Undervoltage lockout with hysteresis
- * Low startup and operating current

ORDERING INFORMATION

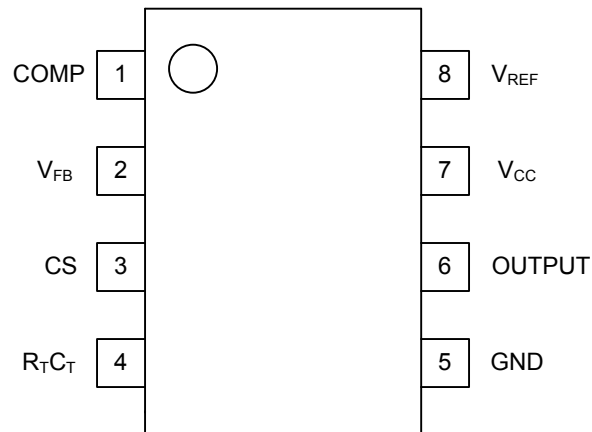
Ordering Number			Package	Packing
Normal	Lead Free	Halogen Free		
UC3842B-D08-T	UC3842BL-D08-T	UC3842BP-D08-T	DIP-8	Tube
UC3842B-S08-R	UC3842BL-S08-R	UC3842BP-S08-R	SOP-8	Tape Reel
UC3843B-D08-T	UC3843BL-D08-T	UC3843BP-D08-T	DIP-8	Tube
UC3843B-S08-R	UC3843BL-S08-R	UC3843BP-S08-R	SOP-8	Tape Reel



Lead-free: UC3842BL
UC3843BL
Halogen-free: UC3842BP
UC3843BP

<p>UC3842BL-D08-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) P: Halogen Free, L: Lead Free, Blank: Pb/Sn</p>
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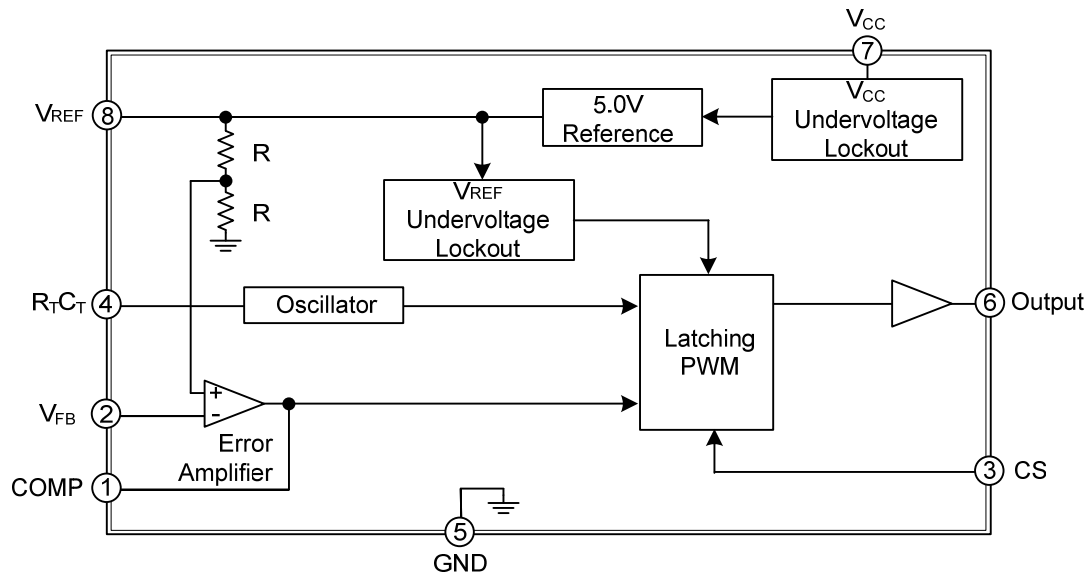
■ PIN CONFIGURATION



■ PIN DESCRIPTIONS

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	COMP	O	Error amp output to provide loop compensation maintaing V_{FB} at 2.5V
2	V_{FB}	I	Error amp inverting input, The non-inverting input of error amp is 2.5V band gap reference
3	CS	I	Current sense input to PWM control gate drive of output
4	$R_T C_T$	I	To set oscillator frequency and maximum output duty cycle
5	GND		Power ground
6	OUTPUT	O	To direct drive power MOSFET
7	V_{CC}		Power supply
8	V_{REF}	O	5V regulated output provides charging current for C_T through R_T

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Total Power Supply and Zener Current	(I _{CC} + I _Z)	30	mA
Output Current, Source or Sink (note1)	I _O	1.0	A
Output Energy (capacitive load per cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V _{IN}	-0.3 ~ +5.5	V
Error Amp. Output Sink Current	I _{O(SINK)}	10	mA
Power Dissipation	DIP-8	1250	mW
	SOP-8	702	mW
Operating Junction Temperature	T _J	+150	°C
Operating Temperature	T _{OPR}	0 ~ +70	°C
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction to Ambient	DIP-8	100	°C/W
	SOP-8	178	°C/W

■ ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, V_{CC}=15V [note 2], R_T=10k, C_T=3.3nF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE SECTION						
Output Voltage	V _{REF}	I _O =1.0mA, T _J =25°C	4.9	5.0	5.1	V
Line Regulation	ΔV _{LINE}	V _{CC} =12V ~ 25V		2.0	20	mV
Load Regulation	ΔV _{LOAD}	I _O =1.0mA ~ 20mA		3.0	25	mV
Temperature Stability	T _S			0.2		mV/°C
Total Output Variation	V _{REF}	Line, Load, Temperature	4.82		5.18	V
Output Noise Voltage	e _N	F=10kHz ~ 10Hz, T _J =25°C		50		μV
Long Term Stability	S	T _A =125°C, 1000Hrs		5		mV
Output Short Circuit Current	I _{SC}		-30	-85	-180	mA
OSCILLATOR SECTION						
Frequency	F	T _J =25°C	49	52	55	kHz
		T _A =0°C ~ 70°C	48		56	
		T _J =25°C (R _T =6.2k, C _T =1.0nF)	225	250	275	
Frequency Change with Voltage	Δf _{OSC} /ΔV	12 ≤ V _{CC} ≤ 25V		0.2	1.0	%
Frequency Change with Temperature	Δf _{OSC} /ΔT	0°C ≤ T _A ≤ 70°C		0.5		%
Oscillator Voltage Swing(Peak to Peak)	V _{OSC}			1.6		V
Discharge Current	I _{dischg}	T _J =25°C	7.8	8.3	8.8	mA
		0°C ≤ T _A ≤ 70°C	7.6		8.8	
ERROR AMPLIFIER SECTION						
Voltage Feedback Input	V _{FB}	V _O =2.5V	2.42	2.50	2.58	V
Input Bias Current	I _{I(BIAS)}	V _{FB} =5.0V		-0.1	-2.0	μA
Open Loop Voltage Gain	G _{VO}	2 ≤ V _O ≤ 4V	65	90		dB
Unity Gain Bandwidth	GB _W	T _J =25°C	0.7	1.0		MHz
Power Supply Rejection Ratio	PSRR	2V ≤ V _{CC} ≤ 25V	60	70		dB
Output Sink Current	I _{SINK}	V _O =1.1V, V _{FB} =2.7V	2.0	12		mA
Output Source Current	I _{SOURCE}	V _O =5.0V, V _{FB} =2.3V	-0.5	-1.0		mA
Output Voltage Swing High State	V _{OH}	V _{FB} =2.3V, R _L =15k to GND	5.0	6.2		V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Swing Low State	V_{OL}	$V_{FB}=2.7V, R_L=15k$ to V_{REF}		0.8	1.1	V
CURRENT SENSE SECTION						
Current Sense Input Voltage Gain	G_V	(Note 3,4)	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold	$V_{I(THR)}$	(Note 3)	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25V$ (Note 3)		70		dB
Input Bias Current	$I_{I(BIAS)}$			-2	-10	μA
Propagation Delay	$t_{D(IN/OUT)}$	Current Sense Input to Output		150	300	ns
OUTPUT SECTION						
Output Low Voltage	V_{OL}	$I_{SINK}=20mA$		0.1	0.4	V
		$I_{SINK}=200mA$		1.6	2.2	V
Output High Voltage	V_{OH}	$I_{SOURCE}=20mA$	13	13.5		V
		$I_{SOURCE}=200mA$	12	13.4		V
Output Voltage with UVLO Activated	$V_{OL(UVLO)}$	$V_{CC}=6.0V, I_{SINK}=1.0mA$		0.1	1.1	V
Output Voltage Rise Time	t_R	$T_J=25^\circ C, C_L=1nF$		50	150	ns
Output Voltage Fall Time	t_F	$T_J=25^\circ C, C_L=1nF$		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION						
Startup Threshold	V_{THR}	UTC UC3842B	14.5	16	17.5	V
		UTC UC3843B	7.8	8.4	9	V
Min. Operating Voltage After Turn-on(V_{CC})	$V_{CC(MIN)}$	UTC UC3842B	8.5	10	11.5	V
		UTC UC3843B	7.0	7.6	8.2	V
PWM SECTION						
Duty Cycle	MAX	DC	94	96		%
	MIN				0	%
Total DEVICE						
Power Startup Supply Current	$I_{CC}+I_C$	$V_{CC}=6.5V$ for UC3843B $V_{CC}=14V$ for UC3842B		0.3	0.5	mA
Power Operating Supply Current	$I_{CC}+I_C$	Note2		12	17	mA
Power Supply Zener Voltage	V_Z	$I_{CC}=25mA$	30	36		V

Note: 1. Maximum Package power dissipation limits must be observed.

2. Adjust V_{CC} above the Startup threshold before setting to 15V.

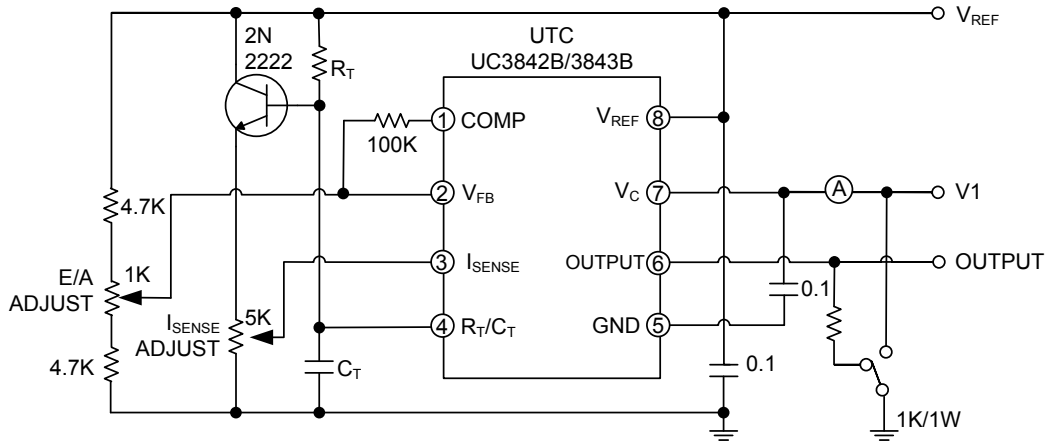
3. This parameter is measured at the latch trip point with $V_{FB}=0V$.

4. Comparator gain is defined as : $G_V = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

TYPICAL APPLICATION CIRCUIT

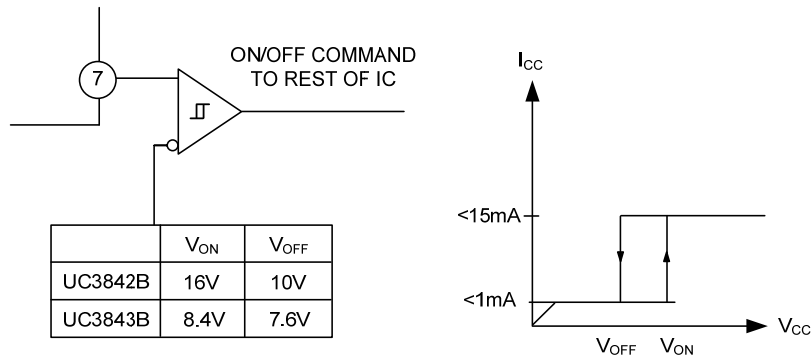
Open Loop Test Circuit

All of the parameters are not all tested in production, although been guaranteed. The timing and bypass capacitors must be connected to pin 5 in a single point ground very closely. To sample the oscillator waveform, the transistor and 5kΩ potentiometer are used, and also can apply an adjustable ramp to I_{SENSE} pin.

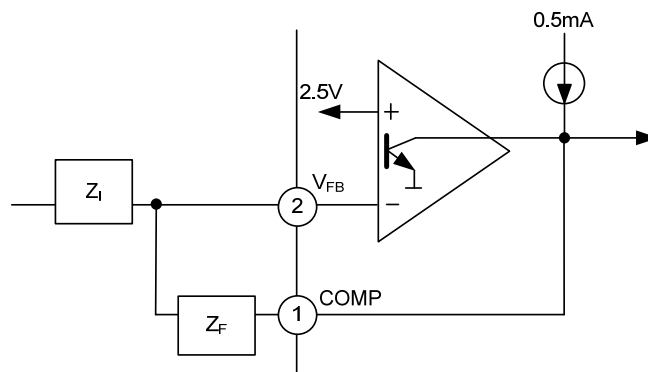


Under Voltage Lockout

Under-Voltage Lock-Out: the output driver is biased to a high impedance state. To prevent activating the power switch with output leakage current, pin 6 should be shunted to ground with a bleeder resistor.



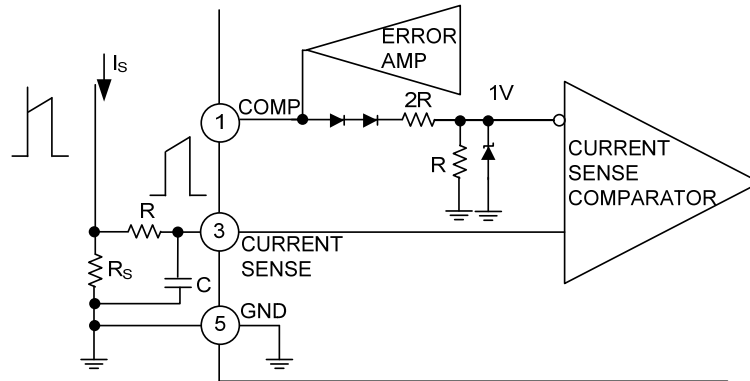
Error Amp Configuration



Error amp can source sink up to 0.5mA

■ APPLICATION INFORMATION(Cont.)

Current Sense Circuit

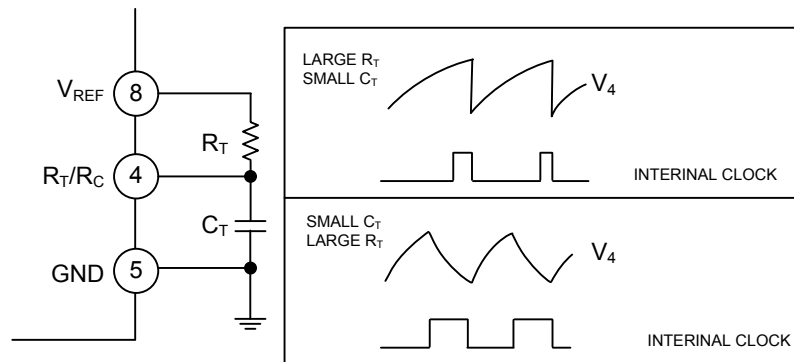


Peak current (I_s) is equaled:

$$I_{S(MAX)} = 1.0V/R_S$$

There should be a small RC filter to suppress switch transients.

Oscillator Waveforms and Maximum Duty Cycle



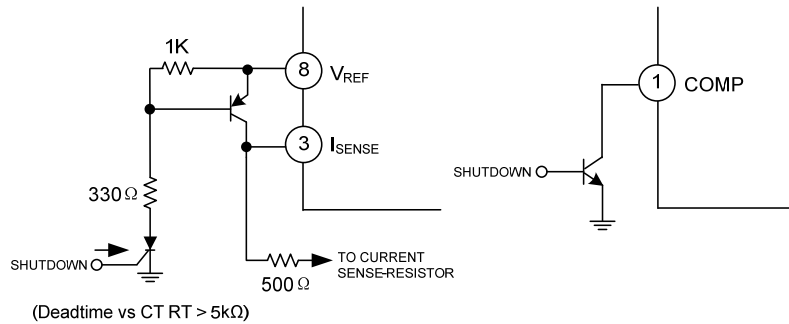
C_T (Oscillator timing capacitor) can be charged by V_{REF} through R_T and discharged by an internal current source. At discharge time, the internal clock signal blanks the output to the low. Both oscillator frequency and maximum duty cycle can be determined by Selection of R_T and C_T . All charge and discharge times can be calculated by the next formulas:

$$t_C = 0.55 R_T C_T$$

$$t_D = R_T C_T I_n \left(\frac{0.0063 R_T - 2.7}{0.0063 R_T - 4} \right)$$

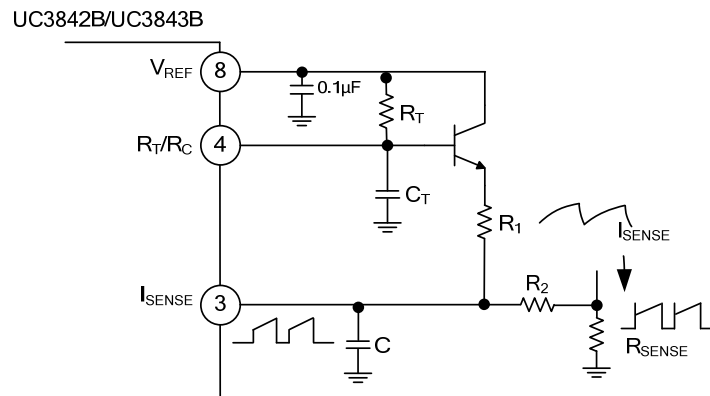
APPLICATION INFORMATION(Cont.)

Shutdown Techniques



The UTC **UC3842B's** shutdown can be accomplished by two ways: raise pin 3 above 1V; or pull pin 1 below a voltage two diode drops above ground. Either method can cause the PWM comparator's output to be high. Because the PWM latch is reset dominant, the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed.

Slope Compensation



TYPICAL CHARACTERISTICS

Figure 1. Timing Resistor Vs. Oscillator Frequency

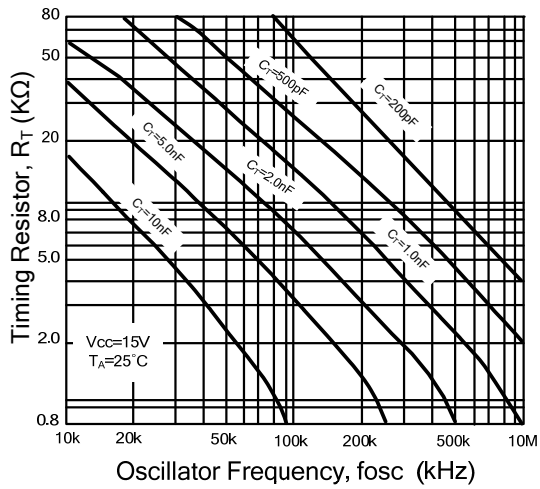


Figure 2. Output Deadtime Vs. Oscillator Frequency

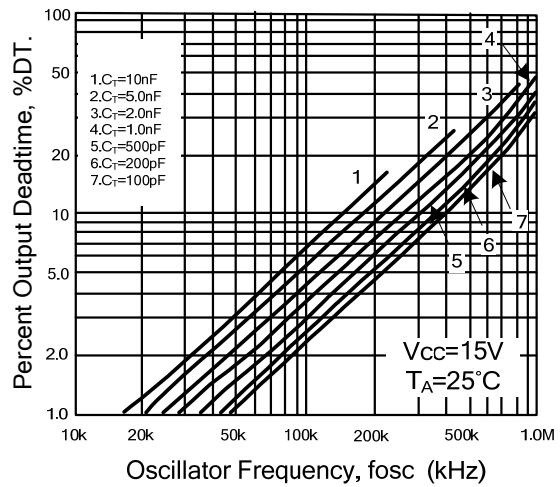


Figure 3. Oscillator Discharge Current Vs. Temperature

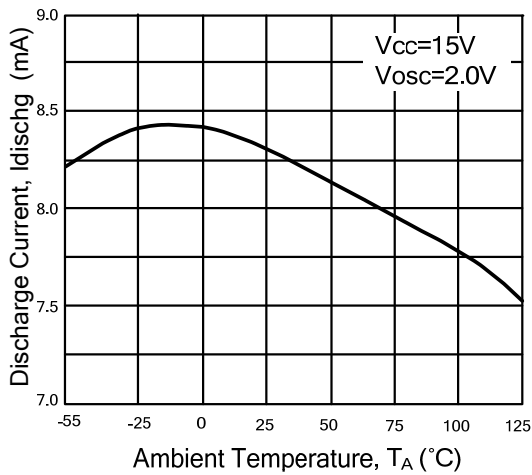


Figure 4. Maximum Output Duty Cycle Vs. Timing Resistor

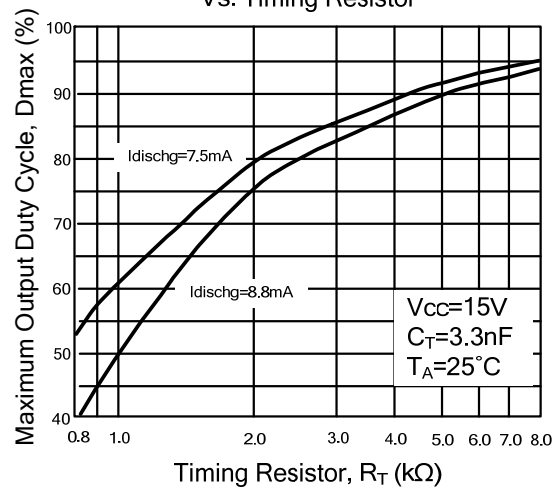


Figure 5. Error Amp Small Signal Transient Response

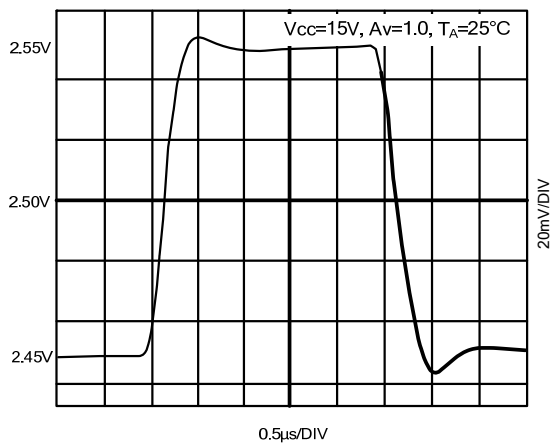
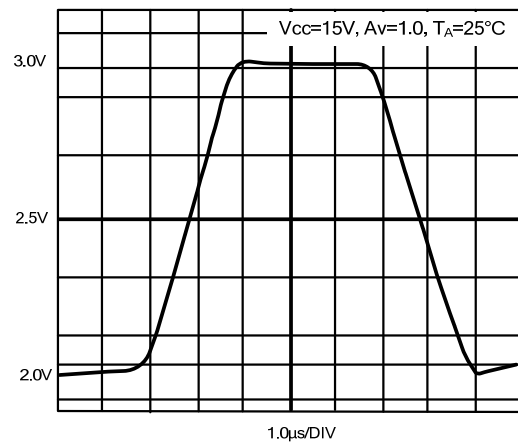


Figure 6. Error Amp Large Signal Transient Response



■ TYPICAL CHARACTERISTICS(Cont.)

Figure 7. Error Amp Open Loop Gain Phase Vs. Frequency

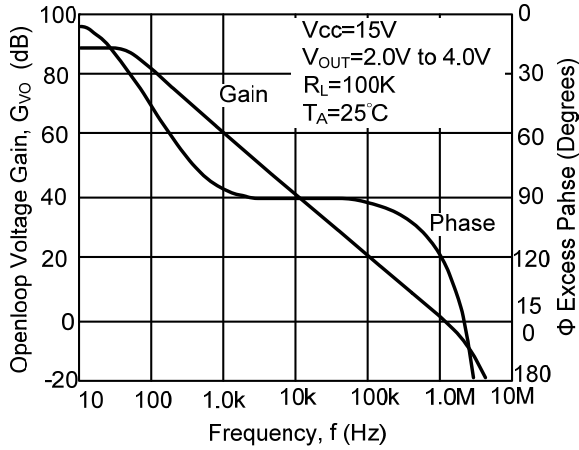


Figure 8. Current Sense Input Threshold Vs. Error Amp Output Voltage

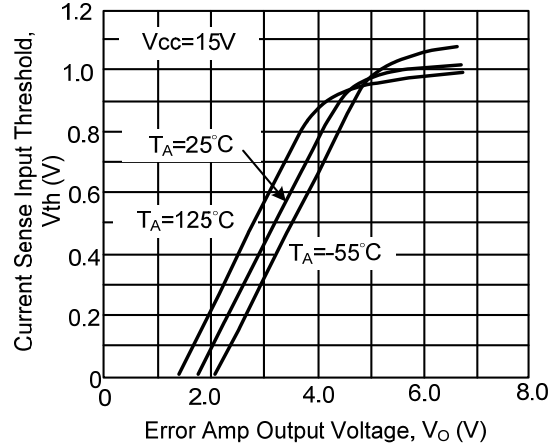


Figure 9. Reference Voltage Change Vs. Source Current

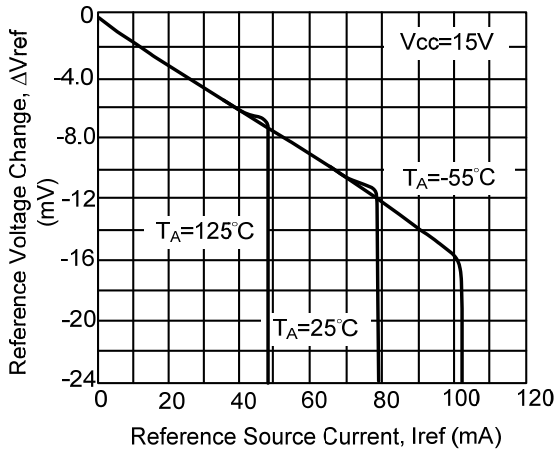


Figure 10. Reference Short Circuit Current Vs. Temperature

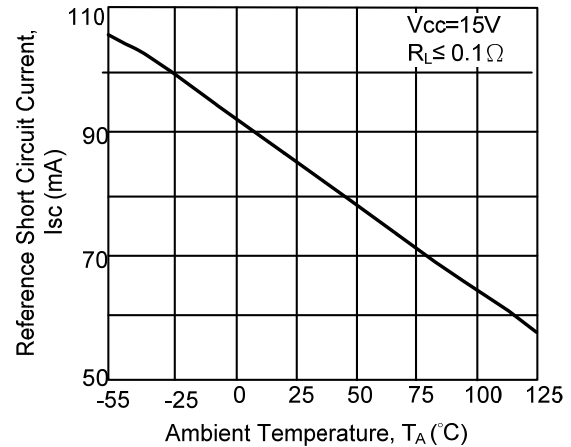


Figure 11. Reference Load Regulation

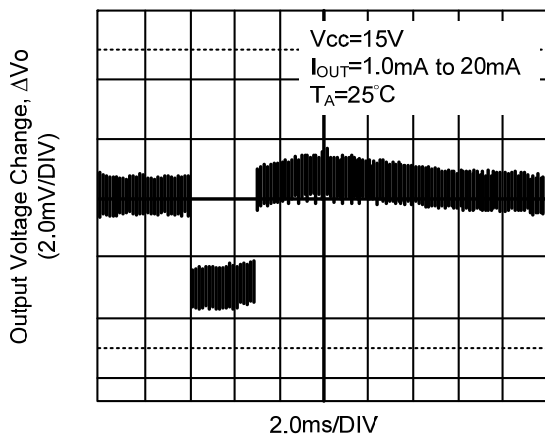
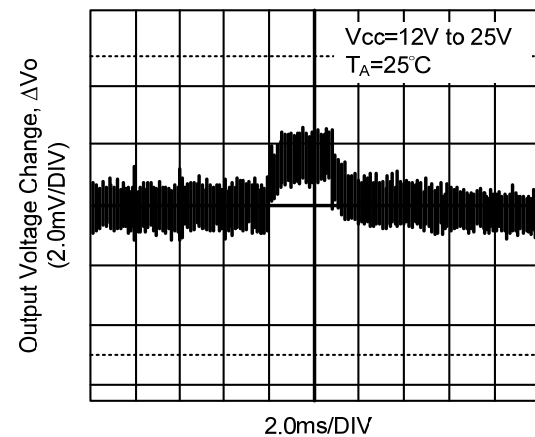


Figure 12. Reference Line Regulation



■ TYPICAL CHARACTERISTICS(Cont.)

Figure 13. Output Saturation Voltage Versus Load Current

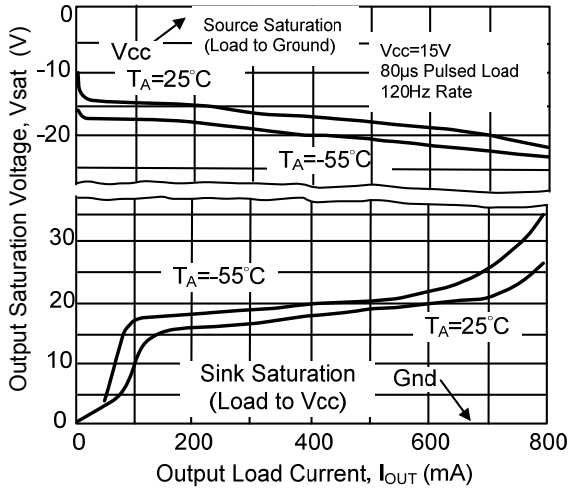


Figure 14. Output Waveform

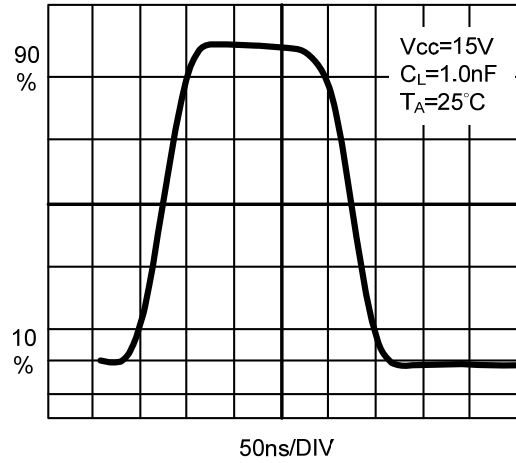


Figure 15. Output Cross Conduction

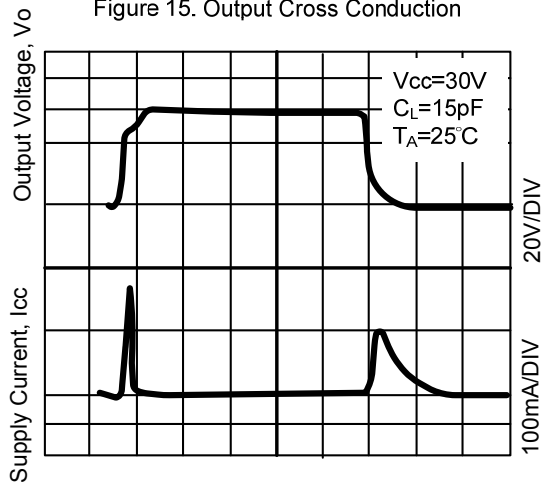
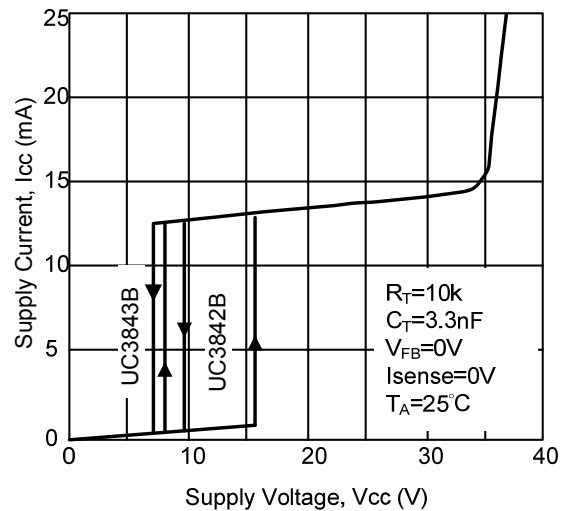


Figure 16. Supply Current vs. Supply Voltage



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