

SN54ABT25244, SN74ABT25244 25-ΩHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992—REVISED OCTOBER 1992

- State-of-the-Art EPIC-II B™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The 'ABT25244 is a 25-Ω octal buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

When the output-enable ($1\overline{OE}$ and $2\overline{OE}$) inputs are low, the device transmits data from the A inputs to the Y outputs. When $1\overline{OE}$ and $2\overline{OE}$ are high, the outputs are in the high-impedance state.

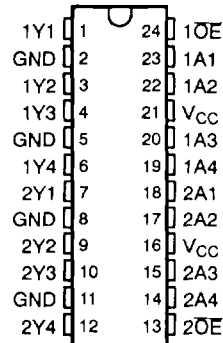
This buffer/driver is capable of sinking 188 mA of I_{OL} current, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

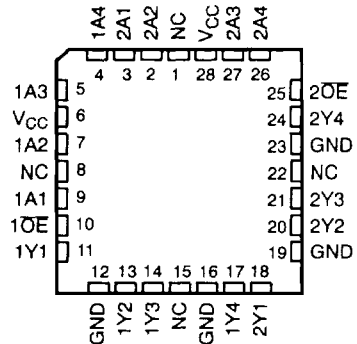
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT25244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT25244 is characterized for operation from -40°C to 85°C .

SN54ABT25244 . . . JT PACKAGE
SN74ABT25244 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ABT25244 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

PRODUCT PREVIEW

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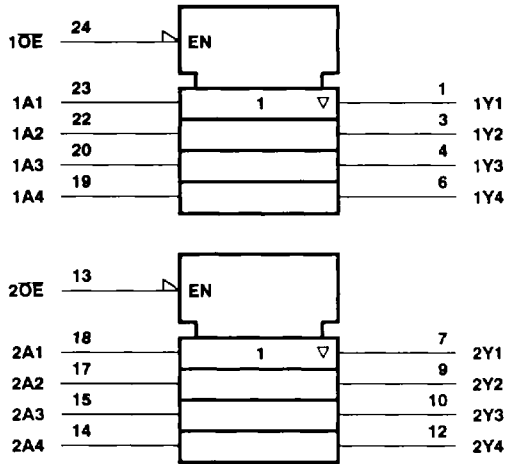
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FUNCTION TABLE
 (each buffer)

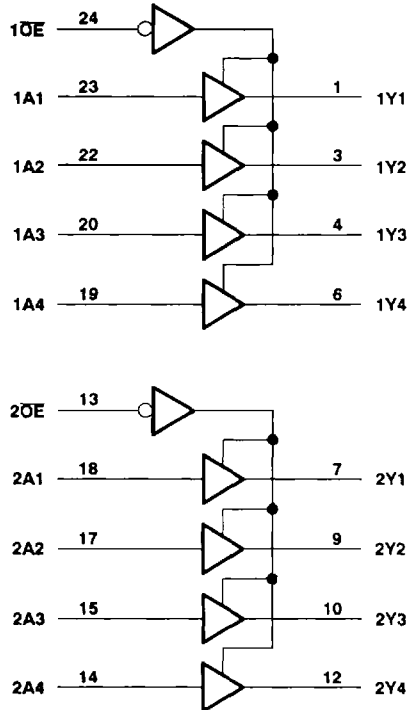
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Current into any output in the low state, I_O : SN54ABT25244	250 mA
SN74ABT25244	376 mA
Operating free-air temperature range: SN54ABT25244	-55°C to 125°C
SN74ABT25244	-40°C to 85°C
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DW package	1 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT25244		SN74ABT25244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{IK}	Input clamp current		-18		-18	mA
I_{OH}	High-level output current		-53		-80	mA
I_{OL}	Low-level output current		125		188	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ABT25244		SN74ABT25244		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	-1.2	V	
V_{OH}	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -3\text{ mA}$			2.7		V	
	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -53\text{ mA}$	2					
	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -80\text{ mA}$			2.4			
V_{OL}	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 94\text{ mA}$		0.55	0.55		V	
	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 125\text{ mA}$		0.8				
	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 188\text{ mA}$			0.7			
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = V_{CC}$ or GND		± 1	± 1		μA	
I_{hold}	$V_{CC} = 4.5\text{ V}$,	$V_I = 0.8\text{ V}$	A pins	100	100		μA	
	$V_{CC} = 4.5\text{ V}$,	$V_I = 2\text{ V}$		-100	-100		μA	
I_{OZH}^\ddagger	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$		50	50		μA	
I_{OZL}^\ddagger	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$		-50	-50		μA	
I_{OFF}	$V_{CC} = 0\text{ V}$,	V_I or $V_O \leq 4.5\text{ V}$		± 500	± 100		μA	
I_{CEX}	$V_{CC} = 5.5\text{ V}$,	$V_O = 5.5\text{ V}$	Outputs high	50	50		μA	
I_O^\S	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.5\text{ V}$		-50	180	-50	180	mA
			Outputs high		500	500	μA	
			Outputs low		30	30	mA	
			Outputs disabled		500	500	μA	
ΔI_{CC}^\ddagger	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V, Other inputs at V_{CC} or GND		1	1		mA	
C_i	$V_{CC} = 5\text{ V}$,	$V_I = V_{CC}$ or GND					pF	
C_o	$V_{CC} = 5\text{ V}$,	$V_O = V_{CC}$ or GND					pF	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

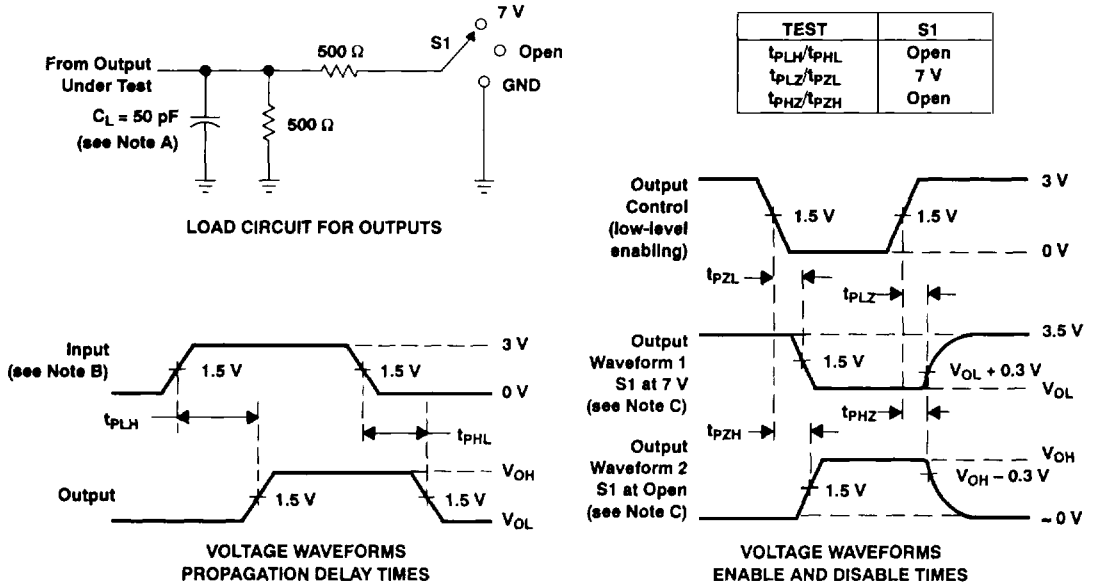
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms