

TYPES SN54ALS574, SN54ALS575, SN54AS574, SN54AS575 SN74ALS574, SN74ALS575, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, JUNE 1982—REVISED DECEMBER 1983

- 3-State Buffer-Type Noninverting Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- 'ALS575 and 'AS575 Have Synchronous Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. The 'ALS575 and 'AS575 may be synchronously cleared by taking the CLR input low.

The output-control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C .

FUNCTION TABLES

'ALS574, 'AS574
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{\text{OC}}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

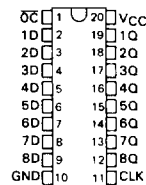
'ALS575, 'AS575
(EACH FLIP-FLOP)

INPUTS				OUTPUT	
$\overline{\text{OC}}$	CLR	CLK	D	Q	
L	L	↑	X	L	L
L	H	↑	H	H	H
L	H	↑	L	L	L
L	H	L	X	Q_0	Q_0
H	X	X	X	Z	Z

SN54ALS574, SN54AS574 . . . J PACKAGE

SN74ALS574, SN74AS574 . . . N PACKAGE

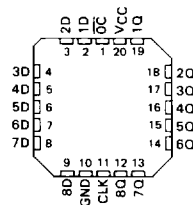
(TOP VIEW)



SN54ALS574, SN54AS574 . . . FH PACKAGE

SN74ALS574, SN74AS574 . . . FN PACKAGE

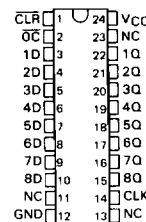
(TOP VIEW)



SN54ALS575, SN54AS575 . . . JT PACKAGE

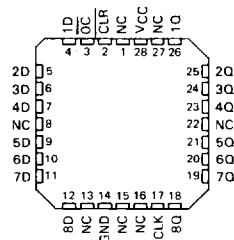
SN74ALS575, SN74AS575 . . . NT PACKAGE

(TOP VIEW)



SN54ALS575, SN54AS575 . . . FH PACKAGE

SN74ALS575, SN74AS575 . . . FN PACKAGE

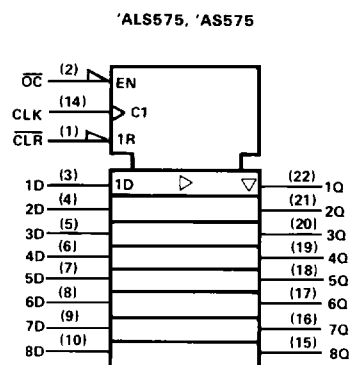
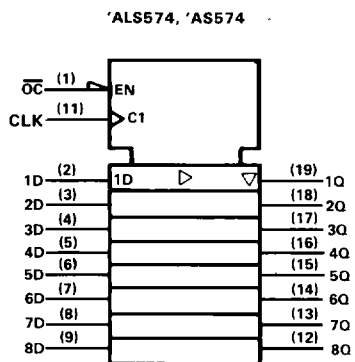


NC — No internal connection

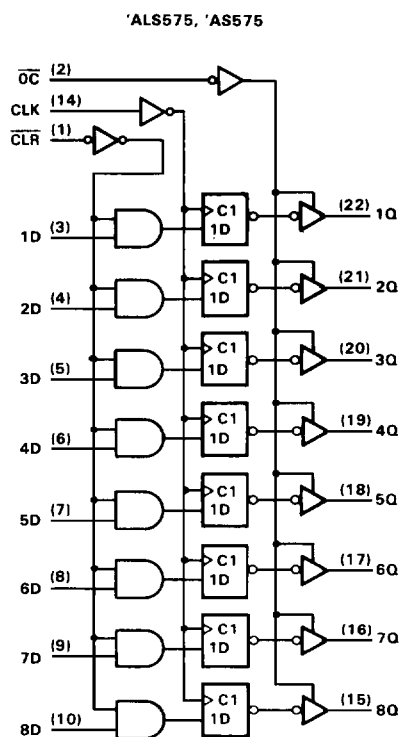
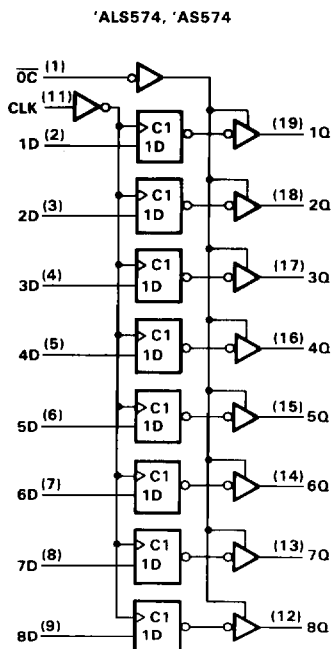
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ALS AND AS CIRCUITS

**TYPES SN54ALS574, SN54ALS575, SN54AS574, SN54AS575
SN74ALS574, SN74ALS575, SN74AS574, SN74AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

logic symbols



logic diagrams (positive logic)



Pin numbers shown are for J and N packages.

Pin numbers shown are for JT and NT packages.

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ALS AND AS CIRCUITS

TYPES SN54ALS574, SN54ALS575, SN74ALS574, SN74ALS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS574, SN54ALS575	-55 °C to 125 °C
SN74ALS574, SN74ALS575	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54ALS574 SN54ALS575			SN74ALS574 SN74ALS575			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V_{IH}	High-level input voltage	2			2			V		
V_{IL}	Low-level input voltage				0.8			V		
I_{OH}	High-level output current				-1			mA		
I_{OL}	Low-level output current				12			mA		
f_{clock}	Clock frequency	'ALS574		0	30		0	MHz		
		'ALS575		0	25		0			
t_w	Pulse duration	'ALS574 CLK high or low		16.5	14		ns			
		'ALS575 CLK high or low		20	16.5					
t_{su}	Setup time before CLK †	Data		15	15		ns			
		'ALS575	CLR high	20	20					
			CLR low	15	15					
t_h	Hold time after CLK †	Data		4	0		ns			
		'ALS575	CLR	0	0					
T_A	Operating free-air temperature	-55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS574 SN54ALS575			SN74ALS574 SN74ALS575			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA				-1.5			V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.4	3.3					
	$V_{CC} = 4.5$ V, $I_{OH} = -2.6$ mA				2.4			
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA	0.25		0.4	0.25		0.4	V
	$V_{CC} = 4.5$ V, $I_{OL} = 24$ mA				0.35		0.5	
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V				20			μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V				-20			μA
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V				0.1			mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V				20			μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V				-0.2			mA
I_O^{\ddagger}	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-15		-70	-15		-70	mA
I_{CC}	$V_{CC} = 5.5$ V	Output high		10	17		mA	
		Outputs low		15	24			
		Outputs disabled		16	27			

†All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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ALS AND AS CIRCUITS

TYPES SN54ALS574, SN54ALS575, SN74ALS574, SN74ALS575

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

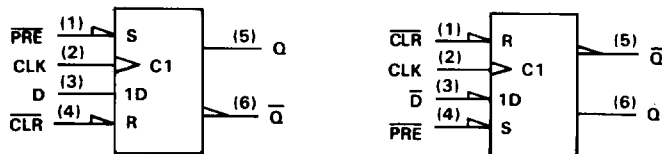
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS574 SN54ALS575		SN74ALS574 SN74ALS575		
			MIN	MAX	MIN	MAX	
f_{max}		'ALS574	30		35		MHz
		'ALS575	25		30		
t_{PLH}	CLK	Any Q	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	OC	Any Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	\overline{OC}	Any Q 'ALS574	2	10	2	8	ns
		Any Q 'ALS575	2	12	2	10	
t_{PLZ}		Any Q	3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called Preset; an input that causes a \overline{Q} output to go high or a Q output to go low is called Clear. Bars are used over these pin names (\overline{PRE} and \overline{CLR}) if they are active low.

In some applications it may be advantageous to redesignate the data input \overline{D} . In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and \overline{Q} exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (\triangle) on \overline{PRE} and \overline{CLR} remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at \overline{D} , Q, and \overline{Q} . Of course pin 5 (\overline{Q}) is still in phase with the data input \overline{D} , but now both are considered active-low.

TYPES SN54AS574, SN54AS575, SN74AS574, SN74AS575

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS574, SN54AS575	-55 °C to 125 °C
SN74AS574, SN74AS575	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			32			48	mA
f_{clock}	Clock frequency	0		100	0		125	MHz
t_w	Pulse duration	CLK high		5	4			ns
		CLK low		3	2			
t_{su}	Setup time before CLK \uparrow	Data		3	2			ns
		'AS575	CLR high or low	6.5	5.5			
t_h	Hold time after CLK \uparrow	Data		3	2			ns
		'ALS575	CLR	0	0			
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS574 SN54AS575		SN74AS574 SN74AS575		UNIT		
		MIN	TYP [†]	MAX	MIN		TYP [†]	MAX
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$		$V_{CC} - 2$		V		
	$V_{CC} = 4.5$ V, $I_{OH} = -12$ mA	2.4	3.2					
	$V_{CC} = 4.5$ V, $I_{OH} = -15$ mA			2.4	3.3			
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 32$ mA	0.29		0.5		V		
	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA			0.34	0.5			
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50		μ A		
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			-50		μ A		
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1		mA		
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20		μ A		
I_{IL}	OC, CLK, CLR			-0.5		mA		
	D			-3				
I_O^{\ddagger}	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-30		-112	-30	-112	mA	
I_{CC}	$V_{CC} = 5.5$ V	Outputs high		73	116	73	116	mA
		Outputs low		85	134	85	134	
		Outputs disabled		84	134	84	134	
		Outputs high		78	126	78	126	
		Outputs low		88	142	88	142	
		Outputs disabled		88	142	88	142	

[†]All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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ALS AND AS CIRCUITS

TYPES SN54AS574, SN54AS575, SN74AS574, SN74AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	\overline{OC}	Any Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	\overline{OC}	Any Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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ALS AND AS CIRCUITS