



**3.3V CMOS  
SINGLE 2-INPUT  
POSITIVE-NAND GATE  
WITH 5 VOLT TOLERANT I/O**

**IDT74LVC1G00A**

**FEATURES:**

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.65mm pitch PSOP package
- Extended commercial range of - 40°C to +85°C
- V<sub>cc</sub> = 3.3V ±0.3V, Normal Range
- V<sub>cc</sub> = 1.65V to 3.6V, Extended Range
- V<sub>cc</sub> = 2.5V ±0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

**Drive Features for LVC1G00A:**

- High Output Drivers: ±24mA
- Reduced system switching noise

**DESCRIPTION:**

This single 2-input positive-NAND gate is built using advanced dual metal CMOS technology. The LVC1G00A is designed for 1.65V to 3.6V V<sub>cc</sub> operation and performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

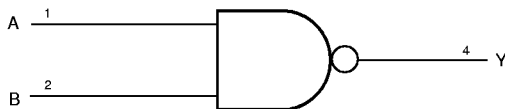
The LVC1G00A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

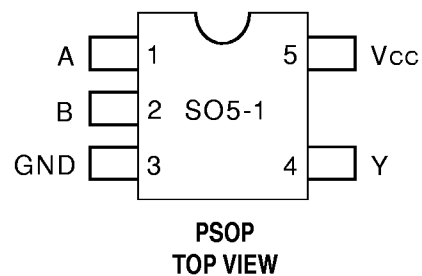
**APPLICATIONS:**

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

**Functional Block Diagram**



**PIN CONFIGURATION**



**PIN DESCRIPTION**

Pin Names	Description
A, B	Data Inputs
Y	Data Output

**FUNCTION TABLE (1)**

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

**NOTE:**

1. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

**ABSOLUTE MAXIMUM RATINGS (1)**

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	- 0.5 to + 6.5	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to + 150	°C
I <sub>OUT</sub>	DC Output Current	- 50 to + 50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

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**CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

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**NOTE:**

1. As applicable to the device type.

**NOTES:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V<sub>CC</sub> terminals.
3. All terminals except V<sub>CC</sub>.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T<sub>A</sub> = - 40°C To +85°C

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 1.65V to 1.95V	0.65 x V <sub>CC</sub>	—	—	V
		V <sub>CC</sub> = 2.3V to 2.7V	1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V	2	—	—	V
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 1.65V to 1.95V	—	—	0.35 x V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3V to 2.7V	—	—	0.7	
		V <sub>CC</sub> = 2.7V to 3.6V	—	—	0.8	
I <sub>IH</sub> I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V		±5	µA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V		±10	µA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = - 18mA		- 0.7	- 1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	mV
I <sub>CCL</sub> I <sub>CCH</sub> I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V	V <sub>IN</sub> = GND or V <sub>CC</sub>		10	µA
			3.6 ≤ V <sub>IN</sub> ≤ 5.5V (2)		10	
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	500	µA

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**NOTE:**

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
2. This applies to 3-state outputs in the disabled state only.

**OUTPUT DRIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 1.65V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 1.65V	I <sub>OH</sub> = -4mA	1.2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -8mA	1.7	—	
		V <sub>CC</sub> = 2.7V	I <sub>OH</sub> = -12mA	2.2	—	
		V <sub>CC</sub> = 3.0V		2.4	—	
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = -24mA	2.2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 1.65V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 1.65V	I <sub>OL</sub> = 4mA	—	0.45	
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 8mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 24mA	—	0.55	
		V <sub>CC</sub> = 3.0V		—	0.55	

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**NOTE:**

- V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = -40°C to +85°C.

**OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C**

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 1.8V±0.15V	V <sub>CC</sub> = 2.5V±0.2V	V <sub>CC</sub> = 3.3V±0.3V	Unit
			Typical	Typical	Typical	
CPD	Power Dissipation Capacitance	CL = 0pF, f = 10Mhz	4.5	4.5	5	pF

**SWITCHING CHARACTERISTICS <sup>(1)</sup>**

Symbol	Parameter	V <sub>CC</sub> = 1.8V±0.15V		V <sub>CC</sub> = 2.5V±0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay	1	12.5	1	6.4	—	5.1	1	4.3	ns
t <sub>PHL</sub>	A or B to Y									

**NOTE:**

- See test circuits and waveforms. T<sub>A</sub> = -40°C to +85°C.

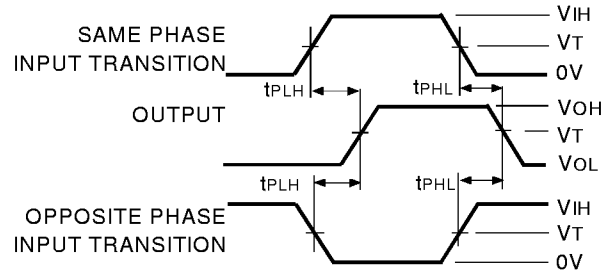
**TEST CIRCUITS AND WAVEFORMS**

**TEST CONDITIONS**

Symbol	V <sub>cc</sub> (1)= 3.3V±0.3V	V <sub>cc</sub> (1)= 2.7V	V <sub>cc</sub> (2)= 2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>cc</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>cc</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>cc</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

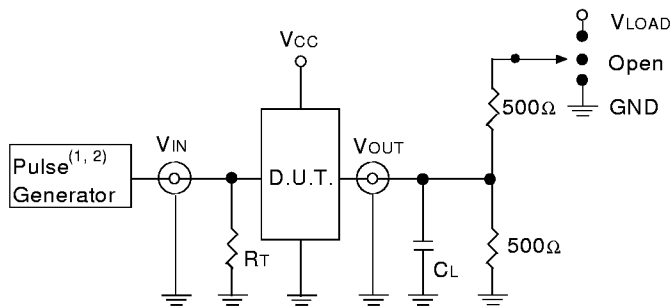
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**PROPAGATION DELAY**



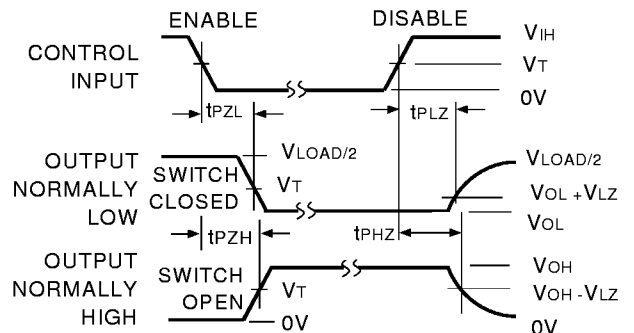
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**TEST CIRCUITS FOR ALL OUTPUTS**



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**ENABLE AND DISABLE TIMES**



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**DEFINITIONS:**

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
 R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

**NOTE:**

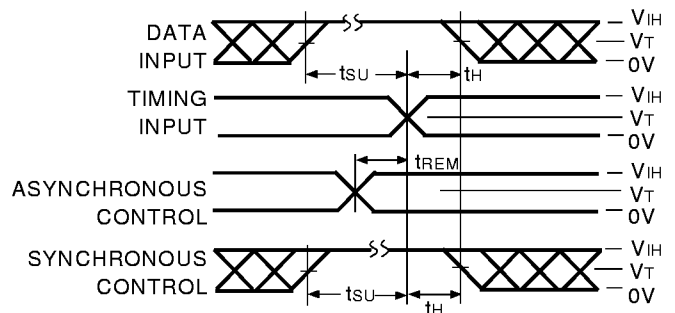
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

**SWITCH POSITION**

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

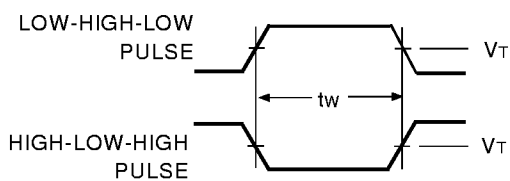
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**SET-UP, HOLD, AND RELEASE TIMES**



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**PULSE WIDTH**



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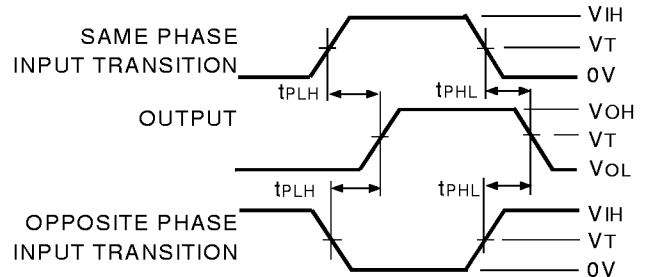
**1.8V ± 0.15V TEST CIRCUITS AND WAVEFORMS**

**TEST CONDITIONS**

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 1.8V ± 0.15V	Unit
V <sub>LOAD</sub>	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	V <sub>CC</sub>	V
V <sub>T</sub>	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	150	mV
V <sub>HZ</sub>	150	mV
C <sub>L</sub>	30	pF

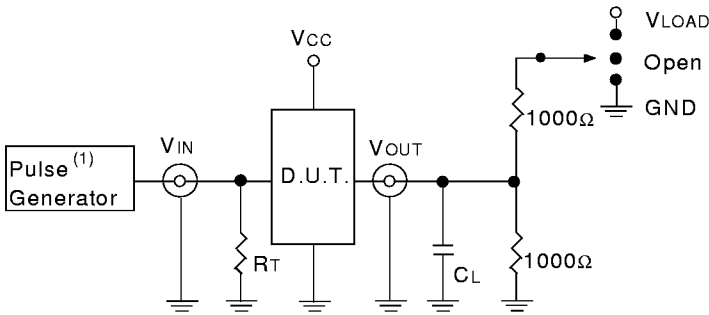
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**PROPAGATION DELAY**



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**TEST CIRCUITS FOR ALL OUTPUTS**



LVC 1G Link

**DEFINITIONS:**

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**NOTE:**

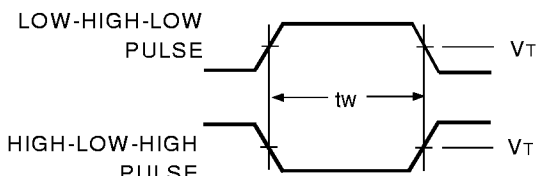
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

**SWITCH POSITION**

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

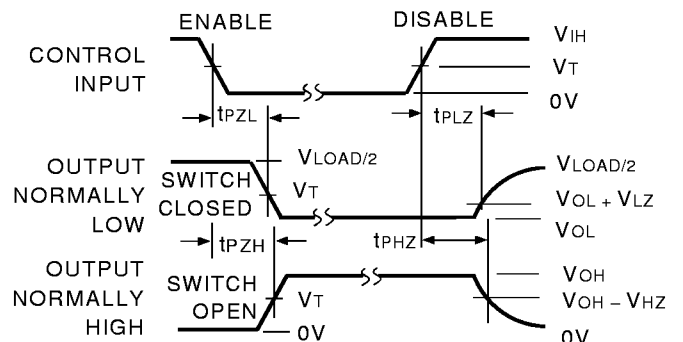
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**PULSE WIDTH**



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**ENABLE AND DISABLE TIMES**

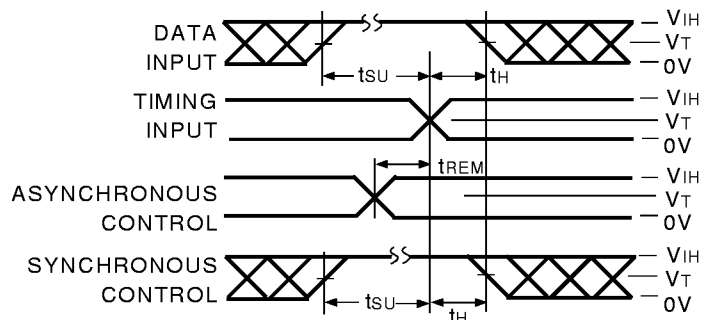


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**NOTE:**

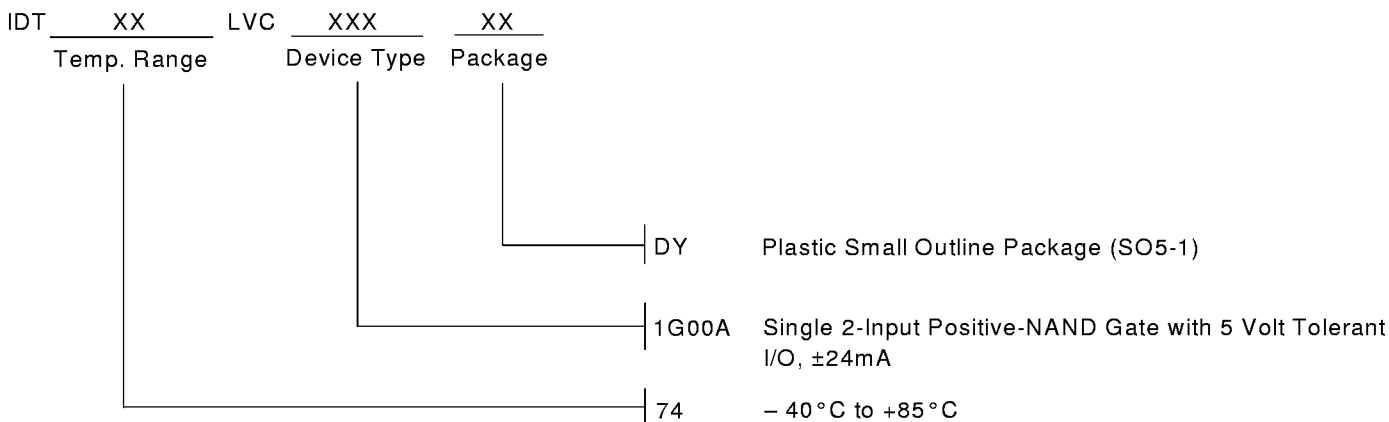
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

**SET-UP, HOLD, AND RELEASE TIMES**



LVC 1G Link

**ORDERING INFORMATION**



**PICOLOGIC-LOGIC (DY) PACKAGES**

Due to their small size, PicoGate-Logic packages require more complex symbolization guidelines. IDT's 5-pin PSOP (DY) packaged devices utilize a three-symbol name rule. The first symbol denotes device technology, the second symbol denotes device function, and the third symbol denotes a wafer fab/assembly site code for internal tracking.

**EXAMPLES:**

1. A PicoGate-Logic device with package code LR\* is an IDT74LVC1G79A.
2. A PicoGate-Logic device with package code GC\* is an IDT74ALVC1G04.

**PICOLOGIC-LOGIC (DY) PACKAGE SYMBOLIZATION GUIDELINES**

TECHNOLOGY	CODE	FUNCTION	CODE
ALVC	G	00	A
ALVCH	J	02	B
LVC	L	04	C
LVCH <sup>(1)</sup>		U04	D
		06 <sup>(1)</sup>	
		07 <sup>(1)</sup>	
		08	E
		14	F
		32	G
		79	R
		86	H
		125	M
		126	N
		132 <sup>(1)</sup>	

**NOTE:**

1. Code to be determined.



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