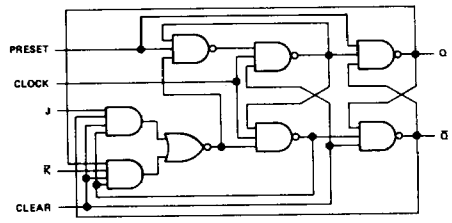
Dual J-K Positive-Edge-Triggered Flip-Flop

DESCRIPTION

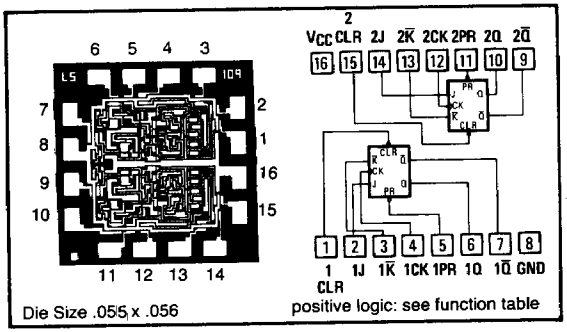
This monolithic dual J-$\overline{K}$ edge-triggered flip-flop features individual J, $\overline{K}$, clock, preset, and clear inputs. A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs.

The J and $\overline{K}$ data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and $\overline{K}$ inputs together.

LOGIC DIAGRAM (½)



PIN-OUT DIAGRAM



Die Size .055 x .056

positive logic: see function table

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: each output changes to the complement of its previous level on each ↑ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$ (High)		17			17			ns
Width of preset pulse, $t_{w(preset)}$ (Low)		15			15			ns
Width of clear pulse, $t_{w(clear)}$ (Low)		15			15			ns
Input setup time t_{setup}		15			15			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the rising edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the clock transition in order to insure recognition. This device requires no hold time.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	J or $\overline{K}$	V_{CC}=MAX, V_I=5.5V				0.1			0.1	mA
	clock or preset					0.2			0.2	
	Clear					0.4			0.4	
I_{IH}	J or $\overline{K}$	V_{CC}=MAX, V_I=2.7V				20			20	μA
	clock or preset					40			40	
	Clear					80			80	
I_{IL}	J or $\overline{K}$	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	clock or preset					−0.8			−0.8	
	Clear					−1.6			−1.6	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX,			4	8		4	8	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5V.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		−55°C			+25°C			+125°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure A on page 2-174)											
t_{PLH}			12	18		10	15		16	23	ns
t_{PHL}	CK Low		22	29		12	18		21	28	ns
	CK High		29	39		16	24		27	38	
t_{PLH}			13	20		12	18		13	20	ns
t_{PHL}			17	27		14	22		15	24	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure A on page 2-174)											
t_{PLH}			16	22		13	19		19	26	ns
t_{PHL}	CK Low		26	33		21	27		24	31	ns
	CK High		33	44		29	38		30	41	ns
t_{PLH}			17	24		15	22		16	25	ns
t_{PHL}			22	31		18	26		19	29	ns

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the rising edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the clock transition in order to insure recognition. This device requires no hold time.

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.