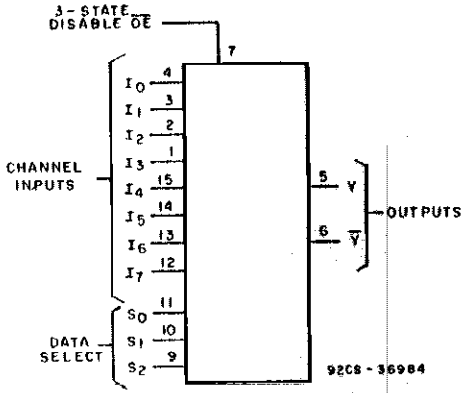
# CD54/74AC251
# CD54/74ACT251




FUNCTIONAL DIAGRAM

## 8-Input Multiplexer, 3-State

**Type Features:**

- *Buffered inputs*
- *Typical propagation delay: 6 ns @ $V_{CC}$ = 5 V, $T_A$ = 25°C, $C_L$ = 50 pF*

The Harris CD54/74AC251 and CD54/74ACT251 8-input multiplexers use the Harris ADVANCED CMOS technology. This multiplexer features both true (Y) and complement ($\overline{Y}$) outputs as well as an Output Enable ($\overline{OE}$) input. The $\overline{OE}$ must be at a LOW logic level to enable this device. When the $\overline{OE}$ input is HIGH, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and $\overline{Y}$ outputs.

The CD74AC251 and CD74ACT251 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC251 and CD54ACT251, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

**Family Features:**

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

**TRUTH TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| SELECT | | | OUTPUT ENABLE $\overline{OE}$ | Y | $\overline{Y}$ |
| S2 | S1 | S0 | | | |
| X | X | X | H | Z | $\overline{Z}$ |
| L | L | L | L | $I_0$ | $\overline{I_0}$ |
| L | L | H | L | $I_1$ | $\overline{I_1}$ |
| L | H | L | L | $I_2$ | $\overline{I_2}$ |
| L | H | H | L | $I_3$ | $\overline{I_3}$ |
| H | L | L | L | $I_4$ | $\overline{I_4}$ |
| H | L | H | L | $I_5$ | $\overline{I_5}$ |
| H | H | L | L | $I_6$ | $\overline{I_6}$ |
| H | H | H | L | $I_7$ | $\overline{I_7}$ |

H = High logic level
L = Low logic level
X = Irrelevant
Z = High impedance (off)
$I_0$, $I_1$ . . . $I_7$ = The level of the respective input

# CD54/74AC251
# CD54/74ACT251

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

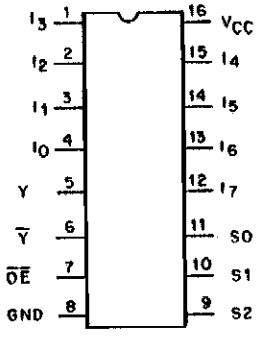
DC SUPPLY-VOLTAGE ($V_{CC}$) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC $V_{CC}$ or GROUND CURRENT ($I_{CC}$ or $I_{GND}$) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For $T_A$ = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55 to +125°C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTICS | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range, $V_{CC}$*: (For $T_A$ = Full Package-Temperature Range) | | | |
| AC Types | 1.5 | 5.5 | V |
| ACT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage, $V_I$, $V_O$ | 0 | $V_{CC}$ | V |
| Operating Temperature, $T_A$ | -55 | +125 | °C |
| Input Rise and Fall Slew Rate, dt/dv | | | |
| at 1.5 V to 3 V (AC Types) | 0 | 50 | ns/V |
| at 3.6 V to 5.5 V (AC Types) | 0 | 20 | ns/V |
| at 4.5 V to 5.5 V (ACT Types) | 0 | 10 | ns/V |

*Unless otherwise specified, all voltages are referenced to ground.




92CS-36831

**TERMINAL ASSIGNMENT**

# CD54/74AC251
# CD54/74ACT251

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | |
| | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | |
| Low-Level Input Voltage $V_{IL}$ | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V |
| | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | |
| | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | #, * | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | #, * | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | #, * | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | #, * | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

# CD54/74AC251
# CD54/74ACT251

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V |
| Low-Level Input Voltage $V_{IL}$ | | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | #, * | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | #, * | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load $\Delta I_{CC}$ | $V_{CC}$-2.1 | | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

### ACT INPUT LOADING TABLE

| INPUT | UNIT LOAD* |
|---|---|
| S0, S1, S3 | 1 |
| OE | 1 |
| $I_0$ - $I_7$ | 1 |

*Unit load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC251
# CD54/74ACT251

**SWITCHING CHARACTERISTICS: AC Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Y Output | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 153 | — | 169 | ns |
| | | 3.3* | 4.9 | 17.2 | 4.7 | 18.9 | |
| | | 5† | 3.5 | 12.3 | 3.4 | 13.5 | |
| Data to $\overline{Y}$ Output | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 169 | — | 186 | ns |
| | | 3.3 | 5.4 | 19 | 5.2 | 20.9 | |
| | | 5 | 3.8 | 13.5 | 3.7 | 14.9 | |
| Select to Y Output | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 207 | — | 228 | ns |
| | | 3.3 | 6.6 | 23.2 | 6.4 | 25.5 | |
| | | 5 | 4.7 | 16.5 | 4.6 | 18.2 | |
| Select to $\overline{Y}$ Output | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 223 | — | 245 | ns |
| | | 3.3 | 7.1 | 24.9 | 6.9 | 27.4 | |
| | | 5 | 5.1 | 17.8 | 4.9 | 19.6 | |
| Output Enable and Output Disable to Output | $t_{PZH}$ $t_{PZL}$ $t_{PHZ}$ $t_{PLZ}$ | 1.5 | — | 155 | — | 169 | ns |
| | | 3.3 | 5.2 | 18.7 | 5.1 | 20.3 | |
| | | 5 | 3.5 | 12.3 | 3.4 | 13.5 | |
| Power Dissipation Capacitance | $C_{PD}$§ | — | 120 Typ. | | 120 Typ. | | pF |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | — | 15 | pF |

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§$C_{PD}$ is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where $f_i$ = input frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage.

**SWITCHING CHARACTERISTICS: ACT Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Y Output | $t_{PLH}$ $t_{PHL}$ | 5† | 3.5 | 12.3 | 3.4 | 13.5 | ns |
| Data to $\overline{Y}$ Output | $t_{PLH}$ $t_{PHL}$ | 5 | 3.8 | 13.5 | 3.7 | 14.9 | ns |
| Select to Y Output | $t_{PLH}$ $t_{PHL}$ | 5 | 4.7 | 16.5 | 4.6 | 18.2 | ns |
| Select to $\overline{Y}$ Output | $t_{PLH}$ $t_{PHL}$ | 5 | 5.1 | 17.8 | 4.9 | 19.6 | ns |
| Output Enable and Output Disable to Output | $t_{PZH}$ $t_{PZL}$ $t_{PHZ}$ $t_{PLZ}$ | 5 | 3.5 | 12.3 | 3.4 | 13.5 | ns |
| Power Dissipation Capacitance | $C_{PD}$§ | — | 120 Typ. | | 120 Typ. | | pF |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | — | 15 | pF |

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§$C_{PD}$ is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where $f_i$ = input frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage.

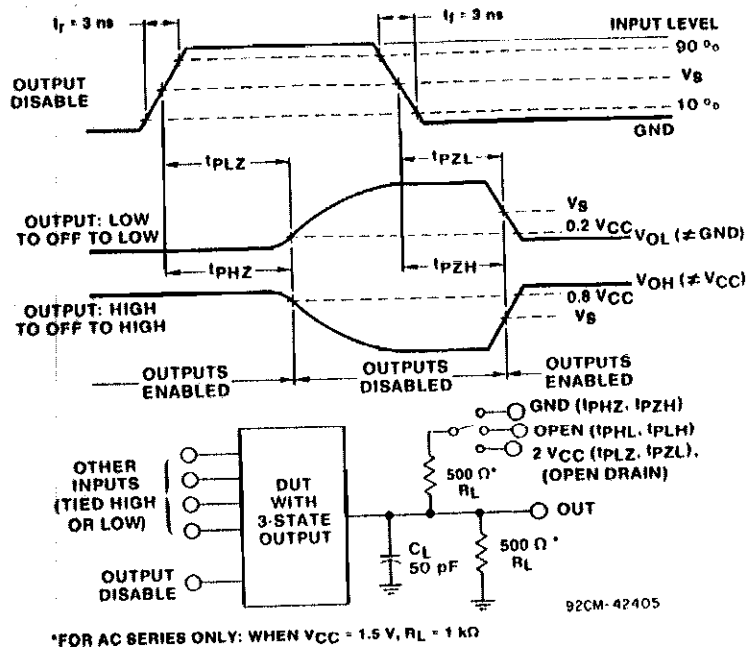
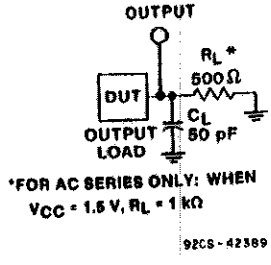



*Fig. 1 - Three-state propagation delay times and test circuit.*



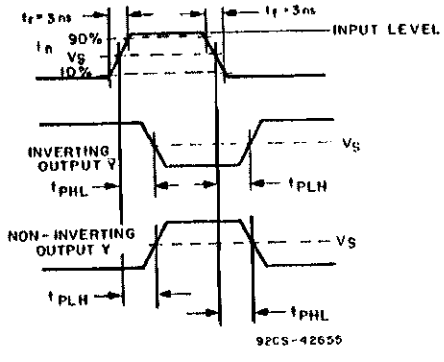




*Fig. 2 - Propagation delay times and test circuit.*

| | CD54/74AC | CD54/74ACT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| Input Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 1.5 V |
| Output Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 0.5 $V_{CC}$ |