



Integrated Device Technology, Inc.

# HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821A/B/C  
IDT54/74FCT823A/B/C  
IDT54/74FCT824A/B/C  
IDT54/74FCT825A/B/C

## FEATURES:

- Equivalent to AMD's Am29821-25 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT821A/823A/824A/825A equivalent to FAST™ speed
- IDT54/74FCT821B/823B/824B/825B 25% faster than FAST
- IDT54/74FCT821C/823C/824C/825C 40% faster than FAST
- Buffered common Clock Enable ( $\overline{EN}$ ) and asynchronous Clear input ( $\overline{CLR}$ )
- $I_{OL} = 48\text{mA}$  (commercial) and  $32\text{mA}$  (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output compatibility
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ( $5\mu\text{A}$  max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

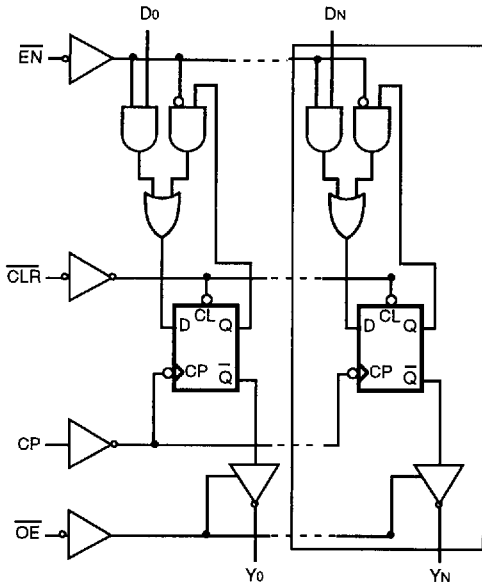
The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821 are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823 and IDT54/74FCT824 are 9-bit wide buffered registers with Clock Enable ( $\overline{EN}$ ) and Clear ( $\overline{CLR}$ ) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825 are 8-bit buffered registers with all the '823 controls plus multiple enables ( $\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$ ) to allow multiuser control of the interface, e.g.,  $\overline{CS}$ , DMA and RD/ $\overline{WR}$ . They are ideal for use as an output port requiring HIGH  $I_{OL}/I_{OH}$ .

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

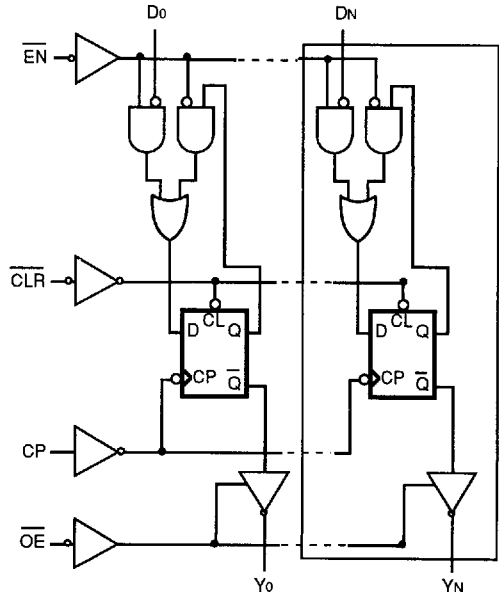
## FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT821/823/825



The IDT logo is a registered trademark of Integrated Device Technology, Inc. 2608 cmv\* 01  
FAST is a trademark of National Semiconductor Co.

IDT54/74FCT824



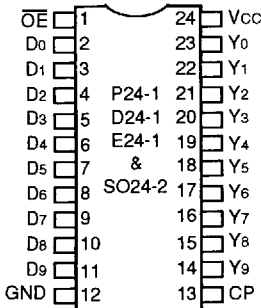
2608 cmv\* 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES

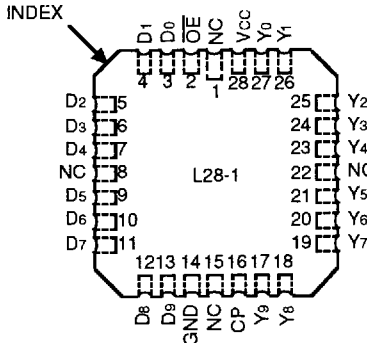
MAY 1992

**PIN CONFIGURATIONS**  
**IDT54/74FCT821 10-BIT REGISTER**

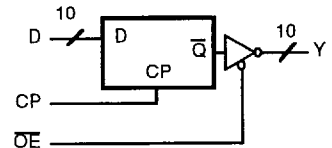
**LOGIC SYMBOLS**



**DIP/SOIC/CERPACK  
TOP VIEW**

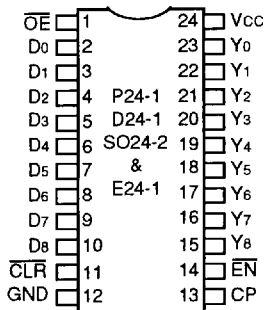


**LCC  
TOP VIEW**

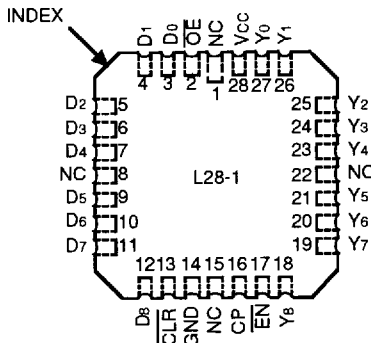


2608 cm\* 03

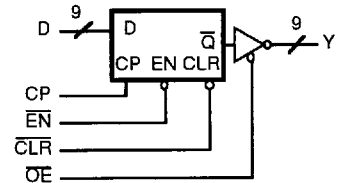
**IDT54/74FCT823/824 9-BIT REGISTERS**



**DIP/SOIC/CERPACK  
TOP VIEW**

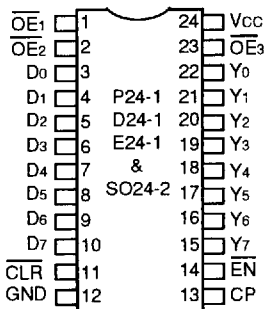


**LCC  
TOP VIEW**

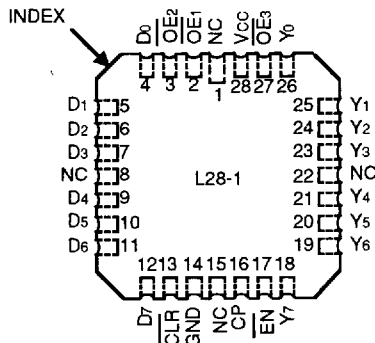


2608 cm\* 04

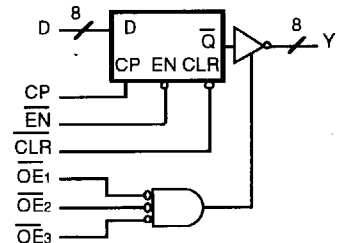
**IDT54/74FCT825 8-BIT REGISTER**



**DIP/SOIC/CERPACK  
TOP VIEW**



**LCC  
TOP VIEW**



2608 cm\* 05

**PRODUCT SELECTOR GUIDE**

	Device		
	10-Bit	9-Bit	8-Bit
Non-inverting	54/74FCT821A/B/C	54/74FCT823A/B/C	54/74FCT825A/B/C
Inverting		54/74FCT824A/B/C	

2608 tbl 01

**PIN DESCRIPTION**

Name	I/O	Description
D <sub>i</sub>	I	The D flip-flop data inputs.
CLR	I	For both inverting and non-inverting registers, when the clear input is LOW and OE is LOW, the Q <sub>i</sub> outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y <sub>i</sub> , $\bar{Y}_i$	O	The register three-state outputs.
EN	I	Clock Enable. When the clock enable is LOW, data on the D <sub>i</sub> input is transferred to the Q <sub>i</sub> output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q <sub>i</sub> outputs do not change state, regardless of the data or clock input transitions.
OE	I	Output Control. When the OE input is HIGH, the Y <sub>i</sub> outputs are in the high impedance state. When the OE input is LOW, the TRUE register data is present at the Y <sub>i</sub> outputs.

2608 tbl 10

**FUNCTION TABLE<sup>(1)</sup>**  
**IDT54/74FCT821/823/825**

Inputs					Internal/Outputs		Function
OE	CLR	EN	D <sub>i</sub>	CP	Q <sub>i</sub>	Y <sub>i</sub>	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

**NOTE:**

2608 tbl 02

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

**FUNCTION TABLE<sup>(1)</sup>**  
**IDT54/74FCT824**

Inputs					Internal/Outputs		Function
OE	CLR	EN	D <sub>i</sub>	CP	Q <sub>i</sub>	Y <sub>i</sub>	
H	H	L	L	↑	H	Z	High Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

**NOTE:**

2608 tbl 03

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub>	-0.5 to V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Input and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

2608 tbl 04

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

- This parameter is measured at characterization but not tested.

2608 tbl 05

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified: V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V  
Commercial: T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5.0V ± 5%; Military: T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit		
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V		
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V		
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max. V <sub>I</sub> = V <sub>CC</sub> V <sub>I</sub> = 2.7V V <sub>I</sub> = 0.5V V <sub>I</sub> = GND	—	—	5	μA		
I <sub>IL</sub>	Input LOW Current		—	—	-5 <sup>(4)</sup>			
I <sub>OZH</sub>	Off State (High Impedance) Output Current		V <sub>O</sub> = V <sub>CC</sub>	—	—		10	μA
I <sub>OZL</sub>			V <sub>O</sub> = 2.7V	—	—		10 <sup>(4)</sup>	
		V <sub>O</sub> = 0.5V	—	—	-10 <sup>(4)</sup>			
		V <sub>O</sub> = GND	—	—	-10			
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>N</sub> = -18mA	—	-0.7	-1.2	V		
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>O</sub> = GND	-75	-120	—	mA		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OH</sub> = -32μA	V <sub>HC</sub>	V <sub>CC</sub>	—	V		
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -300μA	V <sub>HC</sub>	V <sub>CC</sub>	—			
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -15mA MIL.	2.4	4.3	—			
		I <sub>OH</sub> = -24mA COM'L.	2.4	4.3	—			
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OL</sub> = 300μA	—	GND	V <sub>LC</sub>	V		
		V <sub>CC</sub> = Min., I <sub>OL</sub> = 300μA	—	GND	V <sub>LC</sub> <sup>(4)</sup>			
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 32mA MIL.	—	0.3	0.5			
		I <sub>OL</sub> = 48mA COM'L.	—	0.3	0.5			

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2608 tbl 06

**POWER SUPPLY CHARACTERISTICS**

V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open OE = EN = GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle OE = EN = GND One Bit Toggling at f <sub>i</sub> = 5MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.2	6.0	
		V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle OE = EN = GND Eight Bits Toggling at f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	4.0	7.8 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	6.2	16.8 <sup>(5)</sup>	

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

6. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>

I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub> (f<sub>CP</sub>/2 + f<sub>i</sub>N<sub>i</sub>)

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>i</sub> = Input Frequency

N<sub>i</sub> = Number of Inputs at f<sub>i</sub>

All currents are in milliamps and all frequencies are in megahertz.

2608 tbl 07



**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Parameter	Description	Test Conditions <sup>(1)</sup>	IDT54/74FCT821A/ 823A/824A/825A				IDT54/74FCT821B/ 823B/824B/825B				IDT54/74FCT821C/ 823C/824C/825C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay CP to Y <sub>i</sub> (OE = LOW)	CL = 50pF RL = 500Ω	—	10.0	—	11.5	—	7.5	—	8.5	—	6.0	—	7.0	ns
		CL = 300pF <sup>(3)</sup> RL = 500Ω	—	20.0	—	20.0	—	15.0	—	16.0	—	12.5	—	13.5	
tSU	Set-up Time HIGH or LOW D <sub>i</sub> to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW D <sub>i</sub> to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW EN to CP		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW EN to CP		2.0	—	2.0	—	0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{\text{CLR}}$ to Y <sub>i</sub>		—	14.0	—	15.0	—	9.0	—	9.5	—	8.0	—	8.5	ns
tREM	Recovery Time $\overline{\text{CLR}}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$\overline{\text{CLR}}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to Y <sub>i</sub>	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		CL = 300pF <sup>(3)</sup> RL = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	12.5	—	13.5	
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to Y <sub>i</sub>	CL = 5pF <sup>(3)</sup> RL = 500Ω	—	7.0	—	8.0	—	6.5	—	7.0	—	6.2	—	6.2	ns
		CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	7.5	—	8.0	—	6.5	—	6.5	

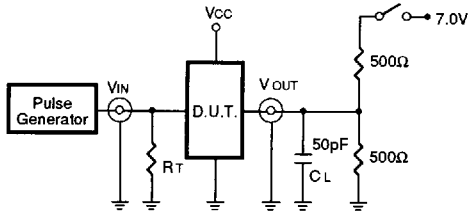
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2698 tbl\* 08

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

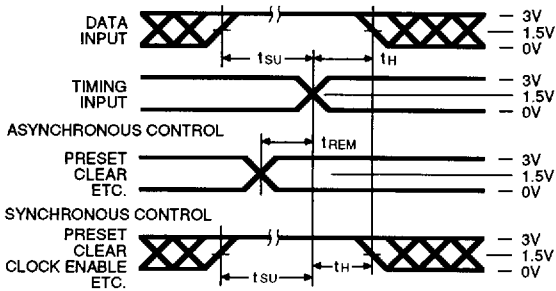
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

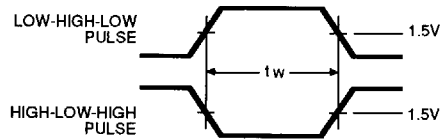
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2608 tbl 09

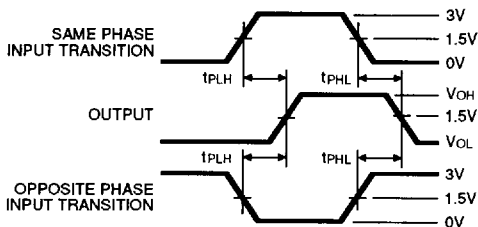
### SET-UP, HOLD AND RELEASE TIMES



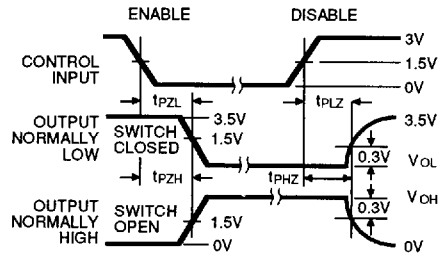
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES



#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz; Zo  $\leq 50\Omega$ ; tr  $\leq 2.5$ ns; tr  $\leq 2.5$ ns.

2608 drw 01

7

**ORDERING INFORMATION**

IDT	XX Temp. Range	FCT	XXXX Device Type	X Package	X Process	
						Blank
						B Commercial MIL-STD-883, Class B
						P Plastic DIP
						D CERDIP
						E CERPACK
						L Leadless Chip Carrier
						SO Small Outline IC
						821A 10-Bit Non-Inverting Register
						821B Fast 10-Bit Non-Inverting Register
						821C Super Fast 10-Bit Non-Inverting Register
						823A 9-Bit Non-Inverting Register
						823B Fast 9-Bit Non-Inverting Register
						823C Super Fast 9-Bit Non-Inverting Register
						824A 9-Bit Inverting Register
						824B Fast 9-Bit Inverting Register
						824C Super Fast 9-Bit Inverting Register
						825A 8-Bit Non-Inverting Register
						825B Fast 8-Bit Non-Inverting Register
						825C Super Fast 8-Bit Non-Inverting Register
						54 -55°C to +125°C
						74 0°C to +70°C

2608 cnv\* 11