HARRIS SEMICONDUCTOR

HCTS109MS

Radiation Hardened Dual $\overline{JK}$ Flip Flop

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Logic Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

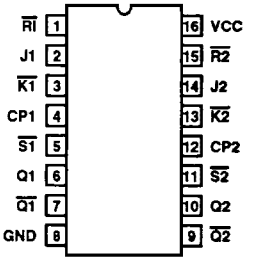
The Harris HCTS109MS is a Radiation Hardened Dual JK Flip Flop with set and reset. The flip flop changes state with the positive transition of the clock (CP1 or CP2).

The HCTS109MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

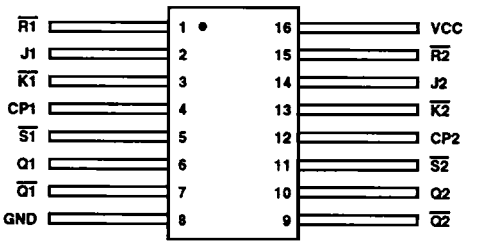
The HCTS109MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW

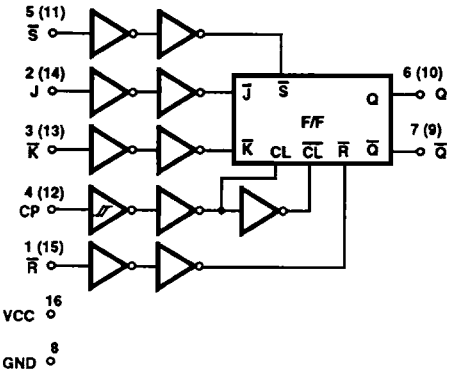


Truth Table

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	Toggle	
H	H	↓	L	H	No Change	
H	H	↓	H	H	H	L
H	H	L	X	X	No Change	

*Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2141.1

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . 100ns/V Max.
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Q, $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	30	ns
	TPHL	VCC = 4.5V	9	+25°C	2	30	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	35	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	23	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 53		pF
			1	+125°C	Typical 53		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	27	MHz
			1	+125°C	-	18	MHz
Setup Time J, K to CP	TSU	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	18	-	ns
Hold Time J, K to CP	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$ to CP	TREM	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	18	-	ns
Pulse Width $\overline{R}$, $\overline{S}$	TW ($\overline{S}$, $\overline{R}$)	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	18	-	ns
Pulse Width $\overline{CP}$	TW (CP)	VCC = 4.5V	1	+25°C	24	-	ns
			1	+125°C	27	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	1.5	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q, $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPHL	VCC = 4.5V	+25°C	2	35	2	44	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	+25°C	2	23	2	29	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	33	2	41	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	+25°C	2	33	2	41	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	33	2	41	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUB-GROUP	DELTA LIMIT
ICC	5	6μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

				OSCILLATOR	
OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
6, 7, 9, 10	1 - 5, 8, 11 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 7, 9, 10	8	-	1 - 5, 11 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8	6, 7, 9, 10	1, 5, 11, 15, 16	4, 12	2, 3, 13, 14

NOTES:

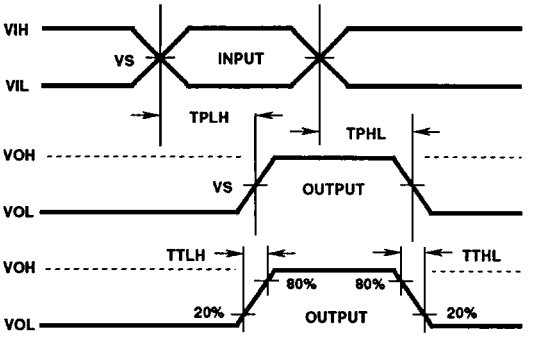
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. RRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 7, 9, 10	8	1, 2, 3, 4, 5, 11, 12, 13, 14, 15, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

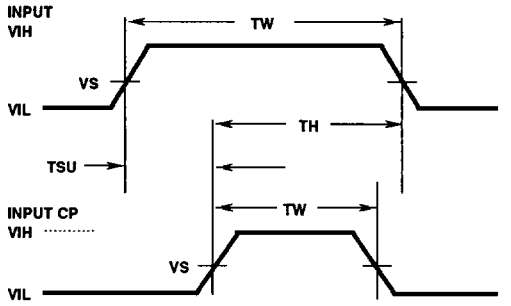
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger

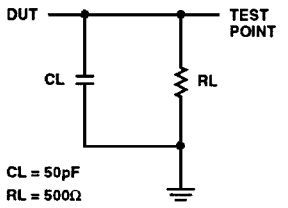


TH = HOLD TIME
TSU = SETUP TIME
TW = PULSE WIDTH

VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25 X 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS109MS