HS-C²MOS™ INTEGRATED CIRCUITS

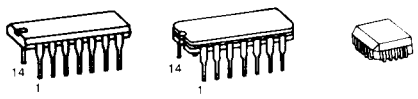
041945

PRELIMINARY DATA

DUAL J-K FLIP-FLOP

DESCRIPTION

The M54/74HC107 is a high speed CMOS DUAL J-K FLIP-FLOP fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These flip-flop are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input. All inputs are equipped with protection circuits against static discharge or transient excess voltage.



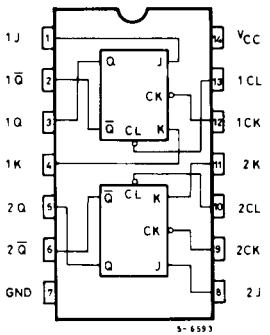
B1 Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS: M54HC107 F1
M74HC107 B1
M74HC107 F1
M74HC107 C1

FEATURES

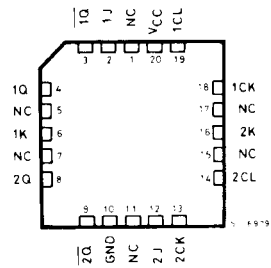
- High Speed
  f_{MAX} = 58 MHz (Typ.) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 2 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 54/74LS107

PIN CONNECTIONS
(top view)



Dual in line

CHIP CARRIER



NC = No Internal Connection

TRUHT TABLE

INPUTS				OUTPUTS	
$\overline{CLEAR}$	$\overline{CLOCK}$	J	K	Q	$\overline{Q}$
L	*	*	*	L	H
H	↓	L	L	NO CHANGE	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	↑	*	*	NO CHANGE	

* : Don't Care ↑ : Transition from Low to High Level
↓ Transition from High to Low Level

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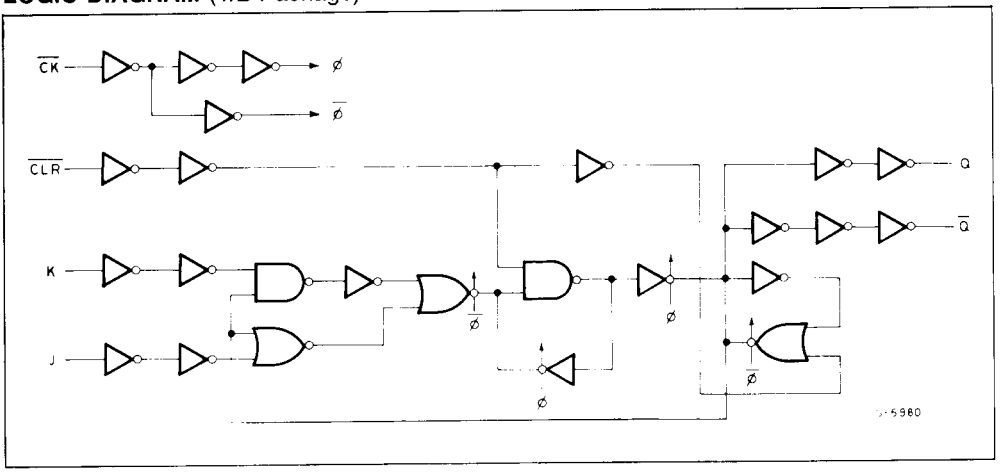
LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5 V	0 to 500	
			V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	2	—	20		40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{CLOCK}$-Q,$\overline{Q}$		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{CLEAR}$-Q,$\overline{Q}$		21	33	ns
f_{MAX}	Maximum Clock Frequency	34	58		MHz
$t_{W(L)}$	Minimum Pulse Width $\overline{CLEAR}$		8	15	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width $\overline{CLOCK}$		8	15	ns
t_s	Minimum Set-up Time		10	20	ns
t_h	Minimum Hold Time		—	0	ns
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$-$\overline{CLOCK}$)		8	15	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{PLH} t_{PHL}	Progataion Delay Time ($\overline{CLOCK}$-Q,$\overline{Q}$)	2.0		—	77	165	—	200			ns
		4.5		—	21	33	—	40			
		6.0		—	18	28	—	34			
t_{PLH} t_{PHL}	Progataion Delay Time ($\overline{CLEAR}$-Q,$\overline{Q}$)	2.0		—	105	195	—	235			ns
		4.5		—	25	39	—	47			
		6.0		—	22	34	—	40			
t_{MAX}	Maximum Clock Frequency	2.0		6	14		5				ns
		4.5		30	50		25				
		6.0		35	58		29				
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0		—	33	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	29	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time	2.0		—	40	100	—	120			ns
		4.5		—	10	20	—	24			
		6.0		—	9	17	—	21			
t_h	Minimum Hold Time	2.0		—	—	0	—	0			ns
		4.5		—	—	0	—	0			
		6.0		—	—	0	—	0			
t_{rem}	Minimum removal Time ($\overline{CLEAR}$ $\overline{CLOCK}$)	2.0		—	16	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance			—	46	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ per F/F