National Semiconductor

54LVQ/74LVQ151
Low Voltage 8-Input Multiplexer

General Description

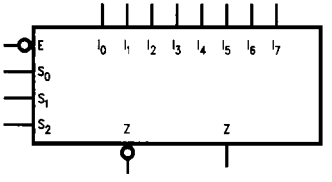
The 'LVQ151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 'LVQ151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code: See Section 8

Logic Symbol



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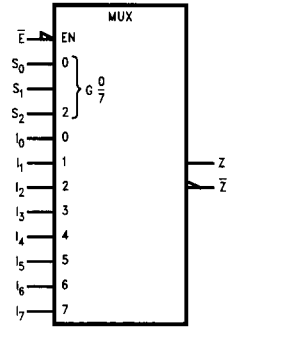
IEEE/IEC



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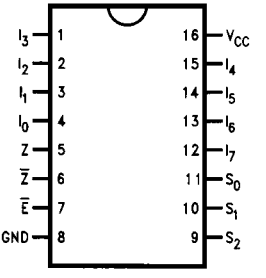
Pin Names	Description
I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\overline{E}$	Enable Input
Z	Data Output
$\overline{Z}$	Inverted Data Output

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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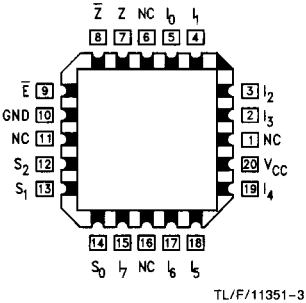
Pin Assignment for LCC



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Truth Table

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

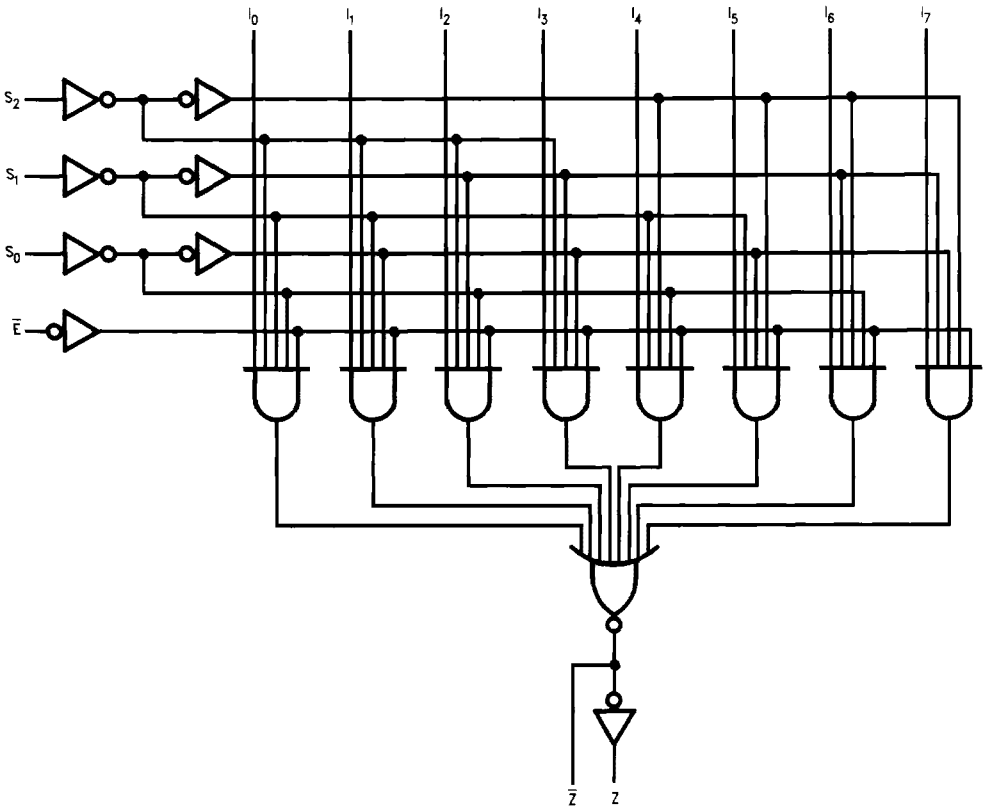
Functional Description

The 'LVQ151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The 'LVQ151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the 'LVQ151 can provide any logic function of four variables and its complement.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	3.0	11.5	18.0	1.0	22.0	3.0	20.0	ns	1.2-3,4
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	2.5	12.0	18.0	1.0	22.0	2.5	20.0	ns	1.2-3,4
t_{PLH}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	2.5	8.0	13.0	1.0	15.5	2.0	14.0	ns	1.2-3,4
t_{PHL}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	1.5	8.5	13.0	1.0	15.5	1.5	14.0	ns	1.2-3,4
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	2.5	9.5	14.0	1.0	16.0	2.0	15.5	ns	1.2-3,4
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	2.5	9.5	15.0	1.0	18.0	2.0	16.0	ns	1.2-3,4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	45	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.