



# Quad 2-Input Positive NOR Buffer

ELECTRICALLY TESTED PER:  
MIL-M-38510/30204

**Military 54LS28**

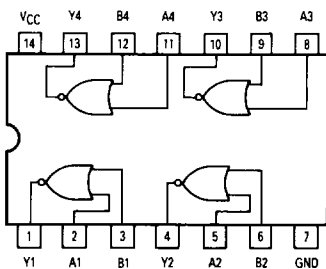


AVAILABLE AS:

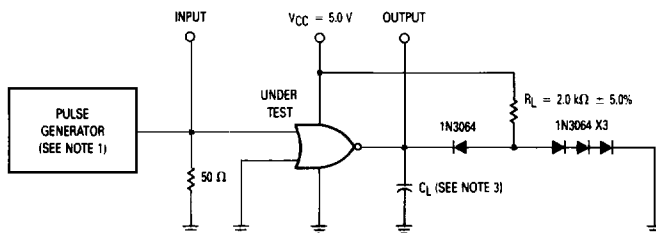
- 1) JAN: JM38510/30204BXA
- 2) SMD: \*
- 3) 883C: 54LS28/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2  
\*Call Factory for latest update

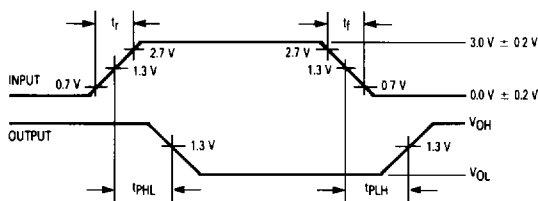
LOGIC DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. Pulse generator has the following characteristics:  $t_r \approx 15$  ns,  $t_f \approx 6.0$  ns,  $PRR \leq 1.0$  MHz,  $t_p = 200 \pm 20$  ns and  $Z_{OUT} = 50 \Omega$ .
2. All diodes are 1N3064 or equivalent.
3.  $C_L = 125$  pF  $\pm 10\%$ , including scope probe, wiring and stray capacitance, without package in test fixture.
4.  $R_L = 667$  k $\Omega \pm 5.0\%$ .
5. Voltage measurements are to be made with respect to network ground terminal.
6. Terminal conditions (pins not designated) may be high  $\geq 2.0$  V, low  $\leq 0.7$  V, or open.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
Y1	1	1	2	VCC
A1	2	2	3	GND
B1	3	3	4	GND
Y2	4	4	6	VCC
A2	5	5	8	GND
B2	6	6	9	GND
GND	7	7	10	GND
A3	8	8	12	GND
B3	9	9	13	GND
Y3	10	10	14	VCC
A4	11	11	16	GND
B4	12	12	18	GND
Y4	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

## 54LS28

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1.2 mA, V <sub>IL</sub> = 0.7 V, other input = 0.7 V.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA, V <sub>IH</sub> = 2.0 V, other input = 0 V.
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other input is open.
I <sub>IH1</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IIN</sub> = 2.7 V, other input = 0 V.
I <sub>IH2</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IIN</sub> = 5.5 V, other input = 0 V.
I <sub>IL</sub>	Logical "0" Input Current	-160	-400	-160	-400	-160	-400	μA	V <sub>CC</sub> = 5.5 V, V <sub>IIN</sub> = 0.4 V, other input = 5.5 V.
I <sub>OS</sub>	Output Short Circuit Current	-30	-130	-30	-130	-30	-130	mA	V <sub>CC</sub> = 5.5 V, V <sub>IIN</sub> = 0 V (all inputs), V <sub>OUT</sub> = 0 V.
I <sub>CCH</sub>	Power Supply Current		3.6		3.6		3.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IIN</sub> = 0 V (all inputs).
I <sub>CCL</sub>	Power Supply Current		13.8		13.8		13.8	mA	V <sub>CC</sub> = 5.5 V, V <sub>IIN</sub> = 5.5 V (all inputs).
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL</sub>	Propagation Delay Data-Output	2.0	25	2.0	30	2.0	30	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 125 pF, R <sub>L</sub> = 667 Ω.
t <sub>PHL</sub>	Propagation Delay Output High-Low		24		30		30	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
t <sub>PLH</sub>	Propagation Delay Data-Output	2.0	25	2.0	30	2.0	30	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 125 pF, R <sub>L</sub> = 667 Ω.
t <sub>PLH</sub>	Propagation Delay Output Low-High		24		30		30	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.

**NOTE:**

1. The limits specified for C<sub>L</sub> = 45 pF are guaranteed but not tested.