Dual 4-Bit Binary Ripple Counter

MC74VHC393

The MC74VHC393 is an advanced high speed CMOS dual 4–bit binary ripple counter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.
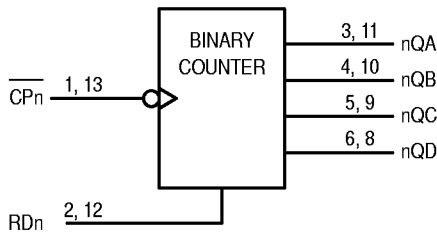
This device consists of two independent 4–bit binary ripple counters with parallel outputs from each counter stage. A ÷256 counter can be obtained by cascading the two binary counters.

Internal flip–flops are triggered by high–to–low transitions of the clock input. Reset for the counters is asynchronous and active–high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the VHC393.

The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: f_{max} = 170MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 236 FETs or 59 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXXD	SOIC
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM

PIN ASSIGNMENT

CP1	1 ●	14	V_{CC}
RD1	2	13	CP2
1QA	3	12	RD2
1QB	4	11	2QA
1QC	5	10	2QB
1QD	6	9	2QC
GND	7	8	2QD

FUNCTION TABLE

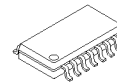| Inputs		Outputs
Clock	**Reset**	
X	H	L
H	L	No Change
L	L	No Change
↑	L	No Change
↓	L	Next State

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MC74VHC393

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage	-0.5 to $+7.0$	V
V_{out}	DC Output Voltage	-0.5 to $V_{CC}+0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating   — SOIC Packages: -7 mW/°C from 65° to 125°C
                      TSSOP Package: -6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		-40	$+85$	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 3.3V$ $V_{CC} = 5.0V$	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25$°C Min	$T_A = 25$°C Typ	$T_A = 25$°C Max	$T_A = -40$ to 85°C Min	$T_A = -40$ to 85°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$			1.50 $V_{CC} \times 0.7$		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 $V_{CC} \times 0.3$		0.50 $V_{CC} \times 0.3$	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
I_{in}	Maximum Input Leakage Current	$V_{in} = 5.5V$ or GND	0 to 5.5			± 0.1		± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0ns$)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$	75 45	120 65		65 35		ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$	125 85	170 115		105 75		
$t_{PLH},$ t_{PHL}	Maximum Propagation Delay, CP to QA	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$		8.6 11.1	13.2 16.7	1.0 1.0	15.5 19.0	ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		5.8 7.3	8.5 10.5	1.0 1.0	10.0 12.0	
$t_{PLH},$ t_{PHL}	Maximum Propagation Delay, CP to QB	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$		10.2 12.7	15.8 19.3	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		6.8 8.3	9.8 11.8	1.0 1.0	11.5 13.5	
$t_{PLH},$ t_{PHL}	Maximum Propagation Delay, CP to QC	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$		11.7 14.2	18.0 21.5	1.0 1.0	21.0 24.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		7.7 9.2	11.2 13.2	1.0 1.0	13.0 15.0	
$t_{PLH},$ t_{PHL}	Maximum Propagation Delay, CP to QD	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$		13.0 15.5	19.7 23.2	1.0 1.0	23.0 26.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		8.5 10.0	12.5 14.5	1.0 1.0	14.5 16.5	
t_{PHL}	Maximum Propagation Delay, RD to Qn	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$		7.9 10.4	12.3 15.8	1.0 1.0	14.5 18.0	ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		5.4 6.9	8.1 10.1	1.0 1.0	9.5 11.5	
$t_{OSLH},$ t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3V$ (Note NO TAG)	$C_L = 50pF$			1.5		1.5	pF
		$V_{CC} = 5.0 \pm 0.5V$ (Note NO TAG)	$C_L = 50pF$			1.0		1.0	pF
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note NO TAG)	23	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$ (per 4–bit counter). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0ns$, $C_L = 50pF$, $V_{CC} = 5.0V$)

Symbol	Parameter	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.5	− 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0ns$)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Typ	$T_A = 25°C$ Limit	$T_A = -40$ to $85°C$ Limit	Unit
t_w	Minimum Pulse Width, CP	$V_{CC} = 3.3 ± 0.3$ V $V_{CC} = 5.0 ± 0.5$ V		5.0 5.0	5.0 5.0	ns
t_w	Minimum Pulse Width, RD	$V_{CC} = 3.3 ± 0.3$ V $V_{CC} = 5.0 ± 0.5$ V		5.0 5.0	5.0 5.0	ns
t_{rec}	Minimum Recovery Time, $\overline{RD}$ to CP	$V_{CC} = 3.3 ± 0.3$ V $V_{CC} = 5.0 ± 0.5$ V		5.0 4.0	5.0 4.0	ns
t_r, t_f	Minimum Input Rise and Fall Times	$V_{CC} = 3.3 ± 0.3$ V $V_{CC} = 5.0 ± 0.5$ V		330 100	330 100	ns

SWITCHING WAVEFORMS
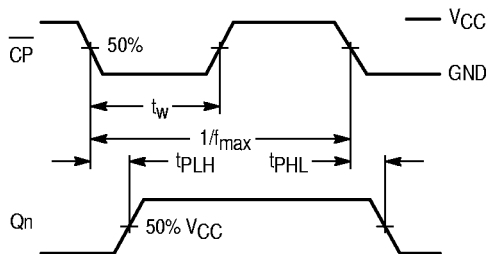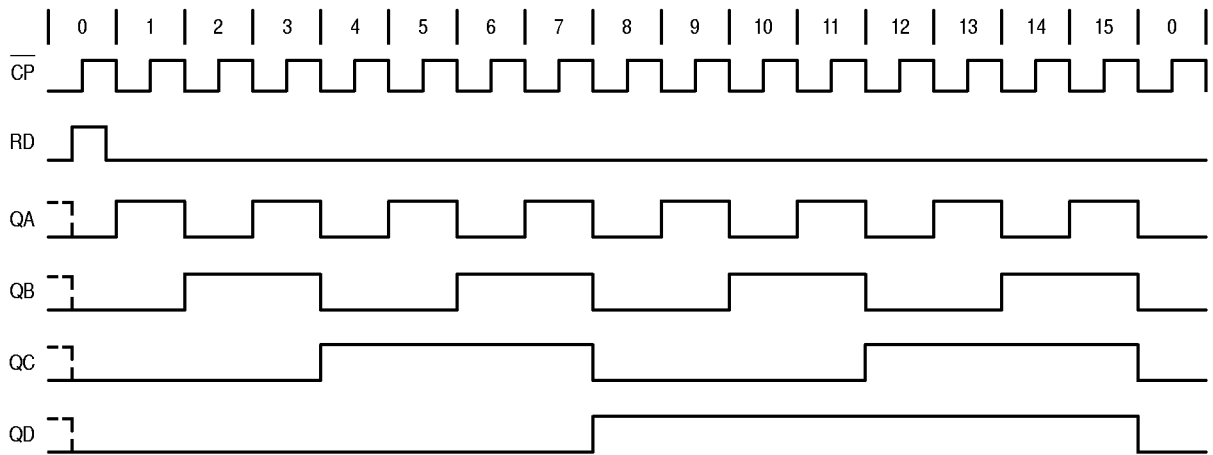

Figure 1.
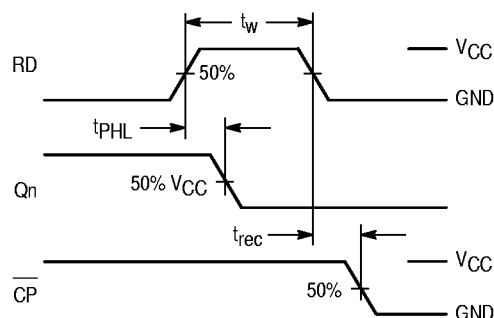
Figure 2.
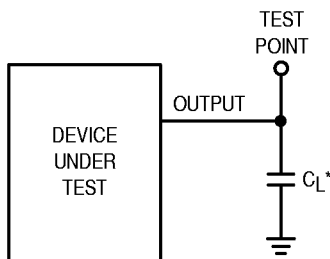
* Includes all probe and jig capacitance

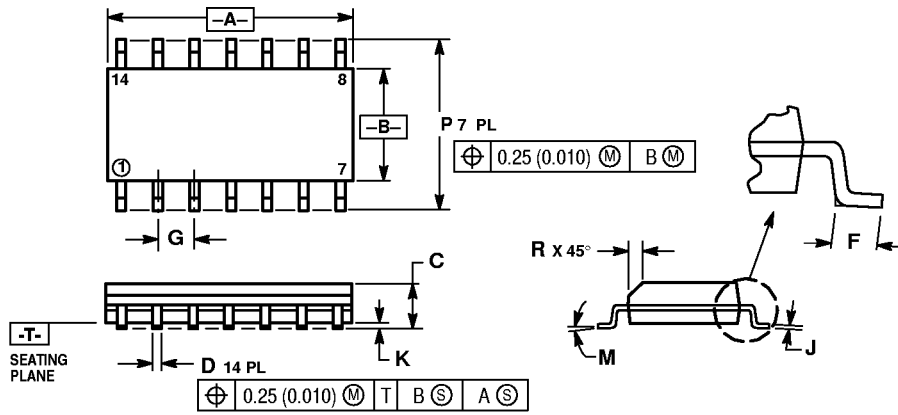Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM
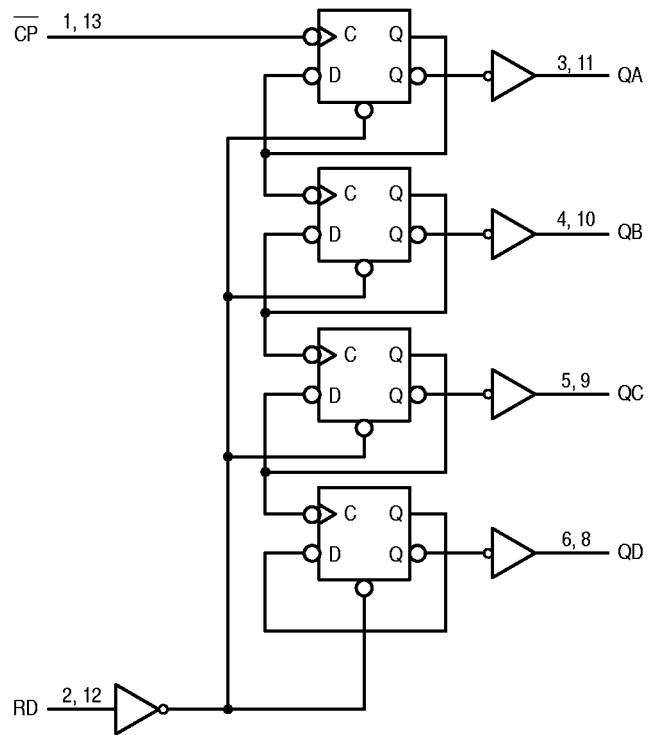
TIMING DIAGRAM

COUNT SEQUENCE

Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

OUTLINE DIMENSIONS

D SUFFIX
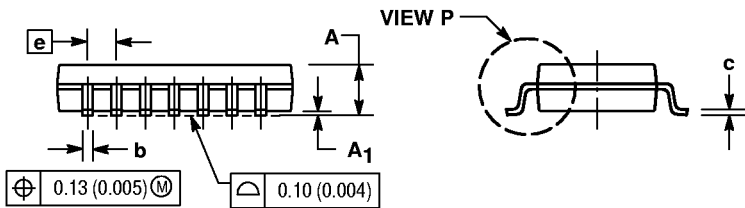### PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
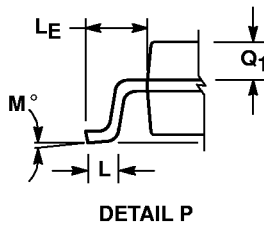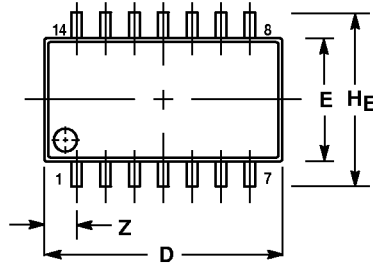### PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O
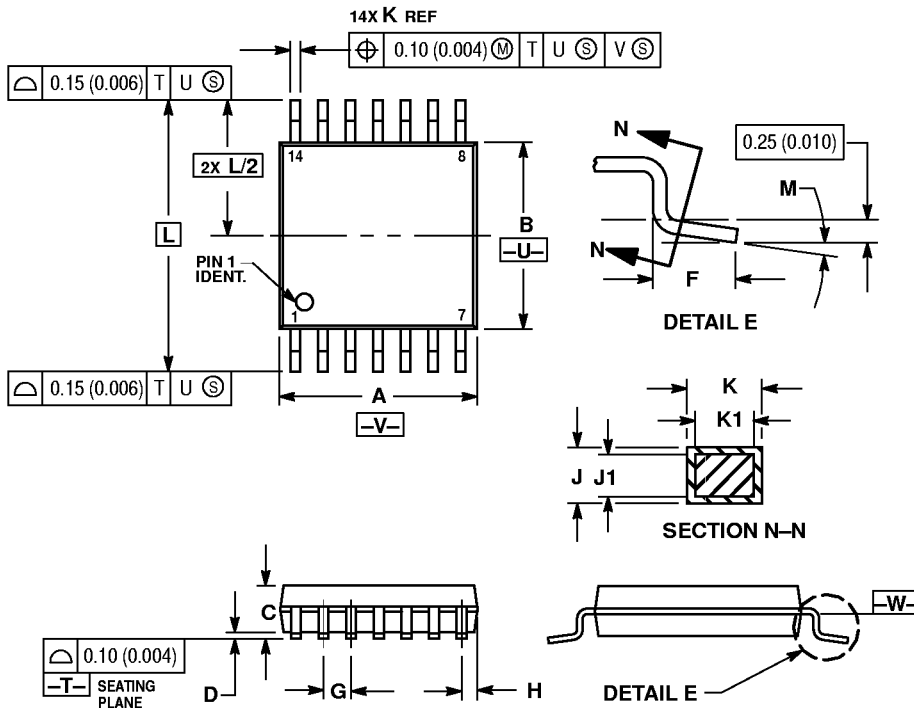
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

OUTLINE DIMENSIONS

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DETAIL P

VIEW P

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

0.13 (0.005) (M)   △ 0.10 (0.004)

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