3.3V CMOS 16-BIT LATCHED TRANSCEIVER

IDT74FCT163543/A/C

FEATURES:

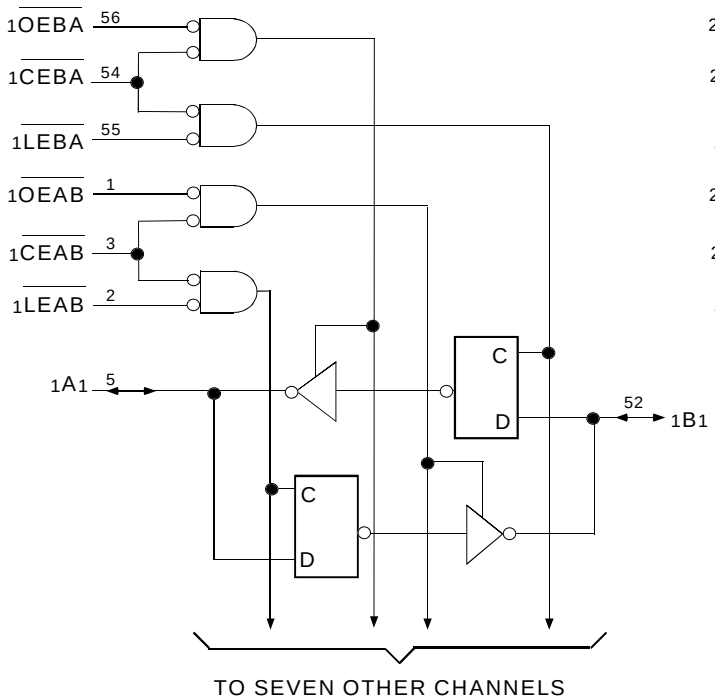
- 0.5 MICRON CMOS Technology
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP Packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

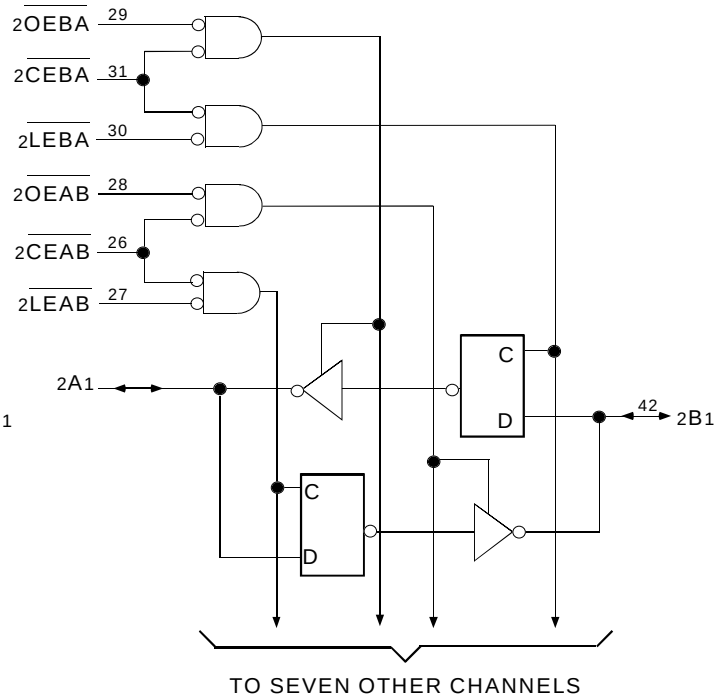
DESCRIPTION:

The FCT163543/A/C 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ($\overline{xCEAB}$) must be low in order to enter data from the A port or to output data from the B port. $\overline{xLEAB}$ controls the latch function. When $\overline{xLEAB}$ is low, the latches are transparent. A subsequent low-to-high transition of $\overline{xLEAB}$ signal puts the A latches in the storage mode. $\overline{xOEAB}$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using $\overline{xCEBA}$, $\overline{xLEBA}$, and $\overline{xOEBA}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163543/A/C have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM





DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = -40°C to +85°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]	Min.	Typ.[2]	Max.	Unit

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} – 0.6V[3]		—	2	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open xCEAB and xOEAB = GND xCEBA = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle xLEAB, xCEAB and xOEAB= GND xCEBA = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1	mA
			V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	0.6	1	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle xLEAB, xCEAB and xOEAB= GND xCEBA = V_{CC} Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4[5]	
			V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	2.4	4.3[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + DI_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

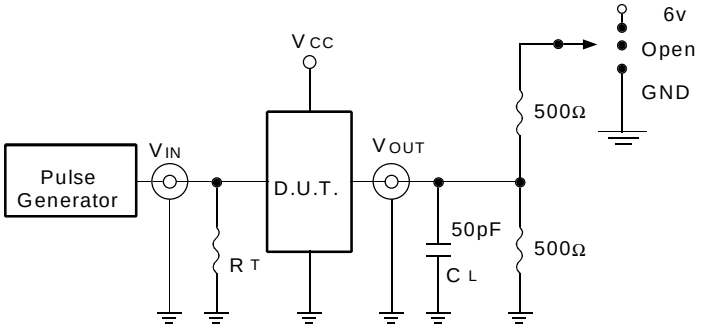
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (4)

Symbol	Parameter	Condition(1)	FCT163543		FCT163543A		FCT163543C		Unit
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	C_L = 50pF R_L = 500Ω	1.5	8.5	1.5	6.5	1.5	5.3	ns
t_{PLH} t_{PHL}	Propagation Delay x$\overline{LEBA}$ to xAx, x$\overline{LEAB}$ to xBx		1.5	12.5	1.5	8	1.5	7	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx		1.5	12	1.5	9	1.5	8	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx		1.5	9	1.5	7.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW xAx or xBx to x$\overline{LEAB}$ or x$\overline{LEBA}$		3	—	2	—	2	—	ns
t_H	Hold Time HIGH or LOW xAx or xBx to x$\overline{LEAB}$ or x$\overline{LEBA}$		2	—	2	—	2	—	ns
t_W	x$\overline{LEBA}$ or x$\overline{LEAB}$ Pulse Width LOW		5	—	5	—	5	—	ns
$t_{SK(o)}$	Output Skew(3)		—	0.5	—	0.5	—	0.5	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

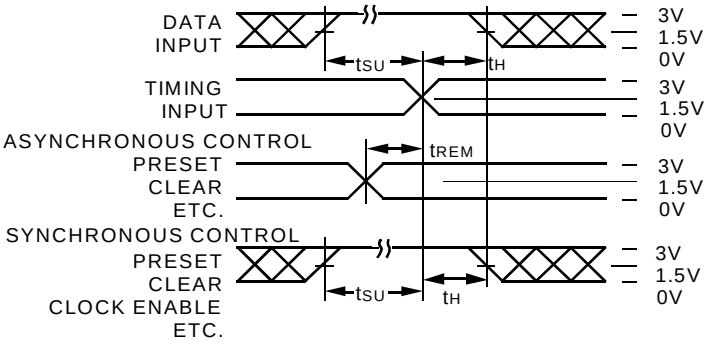
3v16-link

DEFINITIONS:

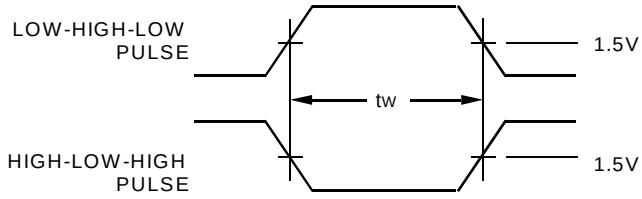
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

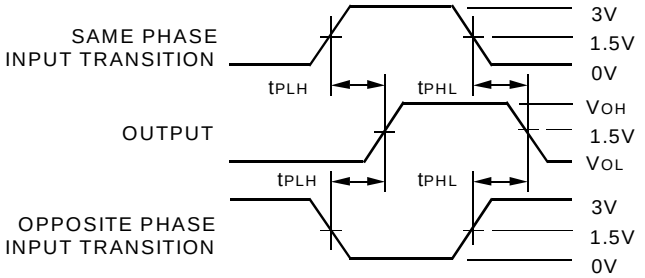
SET-UP, HOLD, AND RELEASE TIMES



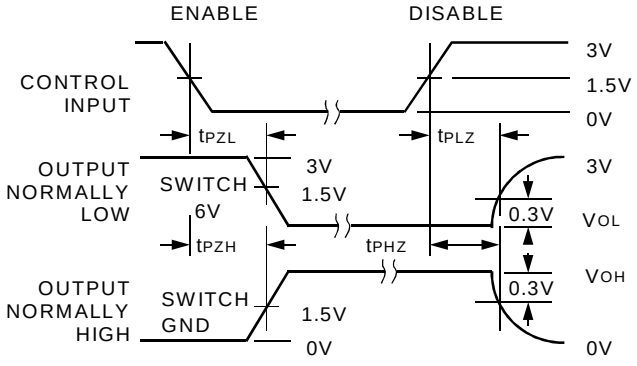
PULSE WIDTH



PROPAGATION DELAY



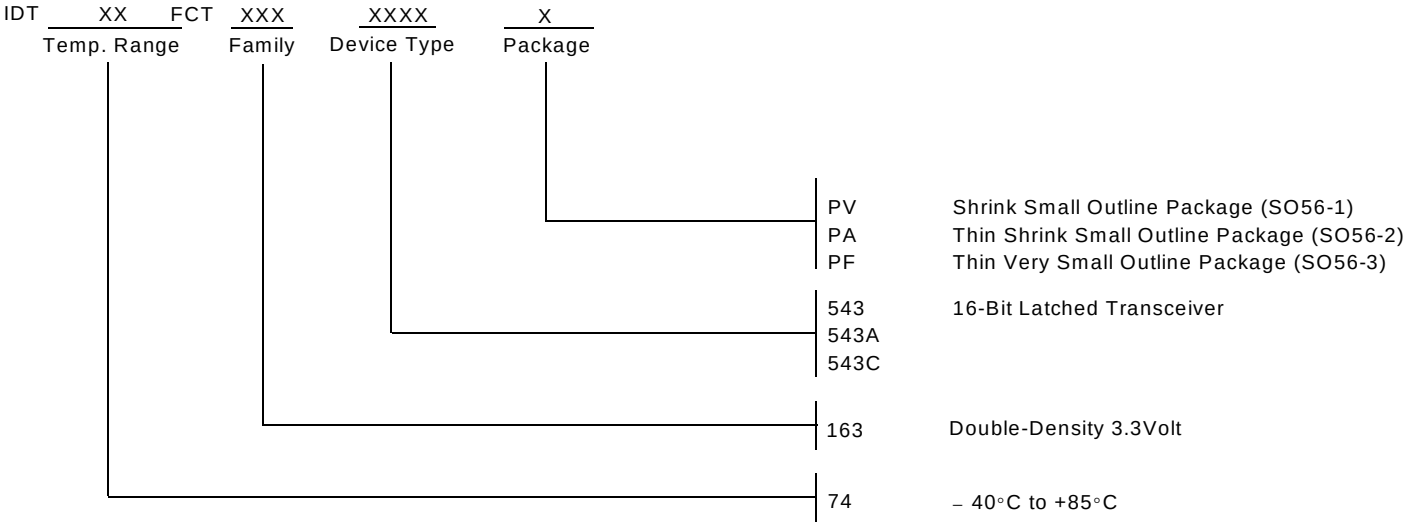
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If Vcc is below 3V, input voltage swings should be adjusted not to exceed Vcc.

ORDERING INFORMATION



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