IH5140-IH5145
High Reliability High-Level CMOS Analog Switch

GENERAL DESCRIPTION

The IH5140 Family of CMOS switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches currently available. These switches can be toggled at a rate of greater than 1MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches combines the speed of the hybrid FET DG180 family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 200pA at 25°C. Very low quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic. It is pin compatible with Intersil's IH5040 family and part of the DG180/190 family as shown in the switching state diagrams.

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	−55°C to 125°C
IH5140 MFD	SPST	14 Pin Flat Pack	−55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	−55°C to 125°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	−55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	−55°C to 125°C
IH5142 MFD	SPDT	14 Pin Flat Pack	−55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	−55°C to 125°C
IH5143 MFD	dual SPDT	14 Pin Flat Pack	−55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	−55°C to 125°C
IH5144 MFD	DPST	14 Pin Flat Pack	−55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	−55°C to 125°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	−55°C to 125°C

Note: 1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

FEATURES

- **Super Fast Break-Before-Make Switching**
- **t_{on} 80ns Typ, t_{off} 50ns Typ (SPST Switches)**
- **Power Supply Currents Less Than 1μA**
- **OFF Leakages Less Than 100pA @ 25°C Typical**
- **Non-latching With Supply Turn-off**
- **Single Monolithic CMOS Chip**
- **Plug-in Replacements for IH5040 Family and Part of the DG180 Family to Upgrade Speed and Leakage**
- **Greater Than 1MHz Toggle Rate**
- **Switches Greater Than 20Vp-p Signals With ±15V Supplies**
- **TTL, CMOS Direct Compatibility**
- **Internal Diode in Series with V^+ for Fault Protection**

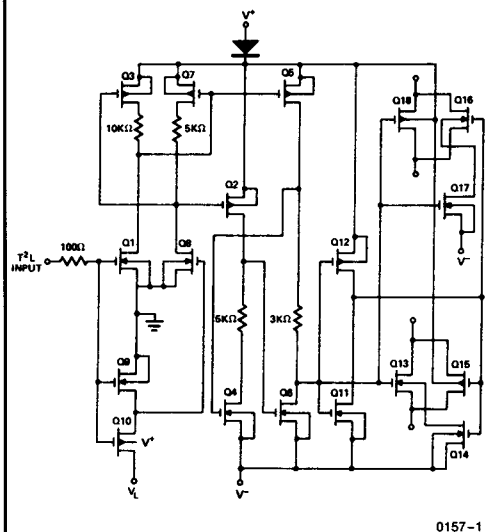


Figure 1: Functional Diagram Typical Driver/ Gate – IH5142

IH5140-IH5145 Family

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <36V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... <33V
$V_L - V_{IN}$ ..... <30V
V_L ..... <20V
V_{IN} ..... <20V

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C

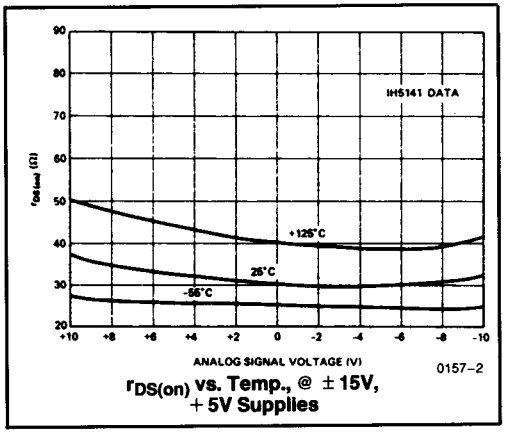
NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

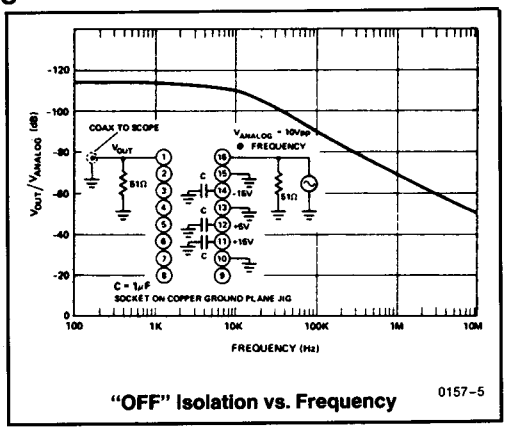
Per Channel		Test Conditions	Min/Max Limits			Units
Symbol	Characteristic		Military			
			−55°C	+25°C	+125°C	
LOGIC INPUT						
I_{INH}	Input Logic Current	$V_{IN} = 2.4V$ Note 1	±1	±1	10	µA
I_{INL}	Input Logic Current	$V_{IN} = 0.8V$ Note 1	±1	±1	10	µA
SWITCH						
$r_{DS(on)}$	Drain–Source On Resistance	$I_S = -10mA$ $V_{ANALOG} = -10V$ to $+10V$	50	50	75	Ω
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match			25 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)		V
$I_{D(off)} + I_{S(off)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$ $V_D = -10V$, $V_S = +10V$		±.5 ±.5	100 100	nA
$I_{D(on)} + I_{S(on)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to $+10V$		±1	200	nA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches See Performance Characteristics		54 (typ)		dB
t_{on} t_{off}	Switch "ON" Time Switch "OFF" Time	See switching time specifications and timing diagrams.				
$Q_{(INJ.)}$	Charge Injection	See Performance Characteristics		10 (typ)		pC
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Performance Characteristics		54 (typ)		dB
SUPPLY						
I^+	+ Power Supply Quiescent Current	$V^+ = +15V$, $V^- = -15V$, $V_L = +5V$ See Performance Characteristics	1.0	1.0	10.0	µA
I^-	− Power Supply Quiescent Current		1.0	1.0	10.0	µA
I_L	+5V Supply Quiescent Current		1.0	1.0	10.0	µA
I_{GND}	Gnd Supply Quiescent Current		1.0	1.0	10.0	µA

NOTES: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

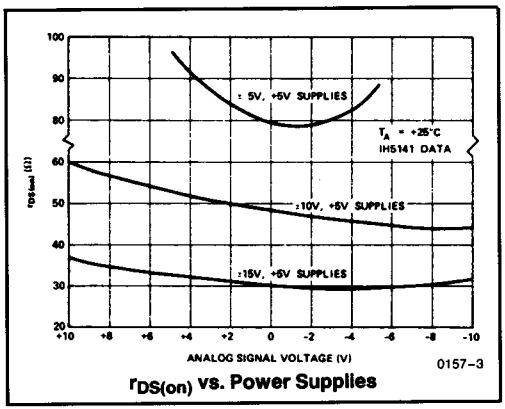
TYPICAL PERFORMANCE CHARACTERISTICS



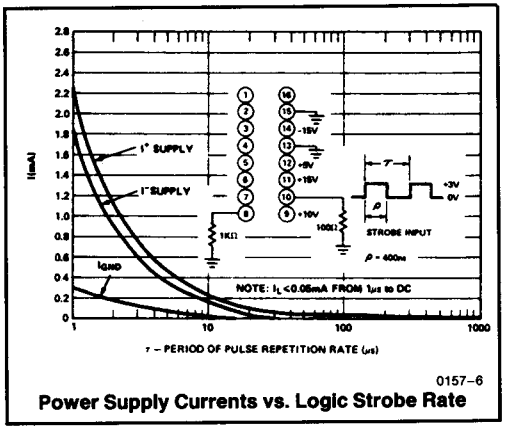
$r_{DS(on)}$ vs. Temp., @ ±15V, +5V Supplies



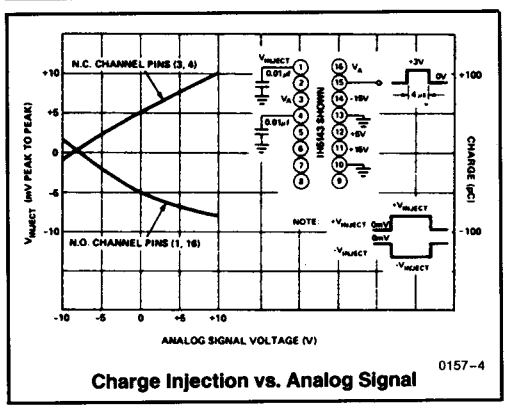
"OFF" Isolation vs. Frequency



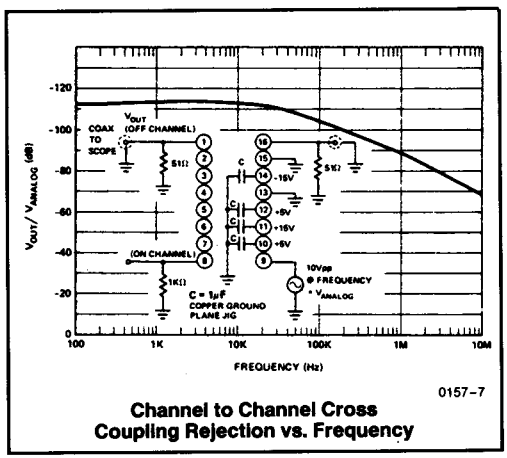
$r_{DS(on)}$ vs. Power Supplies



Power Supply Currents vs. Logic Strobe Rate



Charge Injection vs. Analog Signal



Channel to Channel Cross Coupling Rejection vs. Frequency

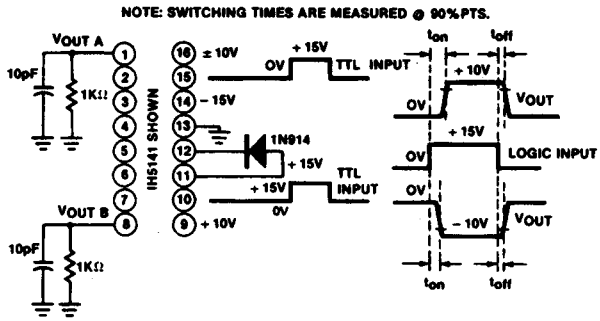
IH5140-IH5145 Family

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

Part Number	Symbol	Characteristic	Test Conditions	Military			Units
				−55°C	+25°C	+125°	
IH5140-5141	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch "OFF" time Break-before-make	Figure 2*		100 75 10		ns
	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch "OFF" time Break-before-make	Figure 3		150 125 *10 (typ)		ns
IH5142-5143	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch 'OFF" time Break-before-make	Figure 2*		175 125 10		ns
	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch "OFF" time Break-before-make	Figure 3		200 125 *10 (typ)		ns
	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch "OFF" time Break-before-make	Figure 4*		175 125 10		ns
	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch "OFF" time Break-before-make	Figure 5*		200 125 10		ns
IH5144-5145	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch "OFF" time Break-before-make	Figure 2*		175 125 10		ns
	t_{on} t_{off} t_{on}-t_{off}	Switch "ON" time Switch "OFF" time Break-before-make	Figure 3		200 125 *10		ns

NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS. * Typical values for design aid only, not guaranteed nor subject to production testing.



0157-8

Figure 2.

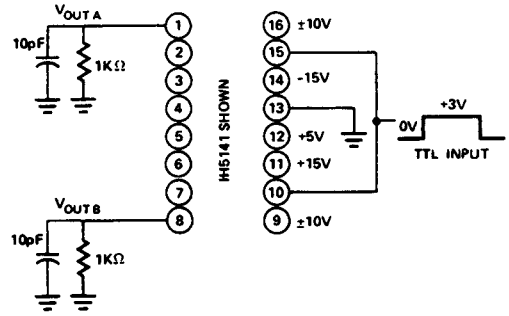


Figure 3.

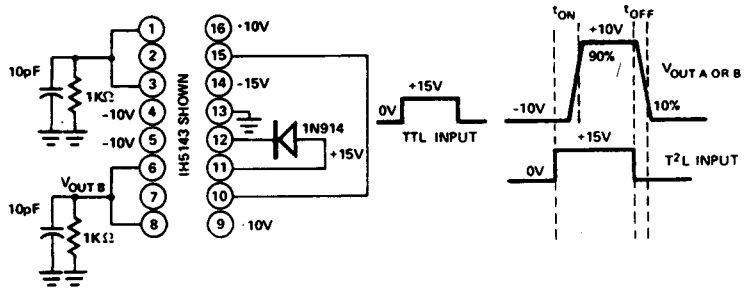


Figure 4.

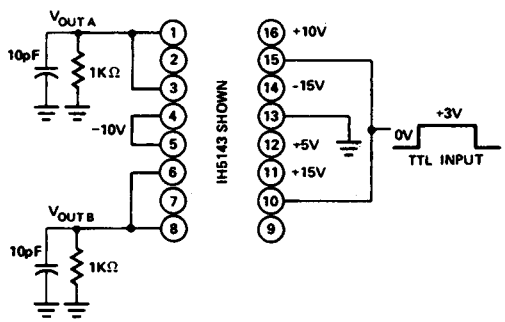
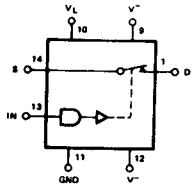


Figure 5.

IH5140–IH5145 Family

FLATPACK (FD-2)



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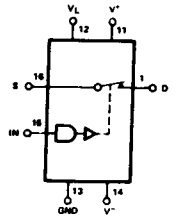
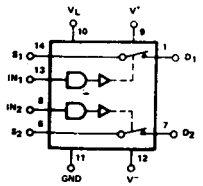
DIP (JE)



0157-13

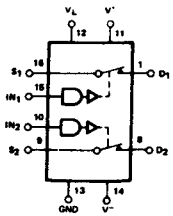
SPST
IH5140 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



0157-14

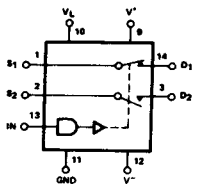
DIP (JE)



0157-15

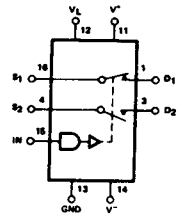
DUAL SPST
IH5141 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



0157-17

DIP (JE)

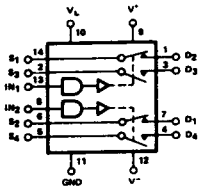


0157-18

SPDT
IH5142 ($r_{DS(on)} < 75\ \Omega$)

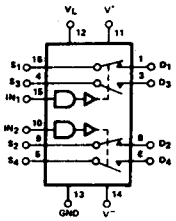
Figure 6: Switching State Diagrams

FLATPACK (FD-2)



0157-20

DIP (JE) (DG191 EQUIVALENT)

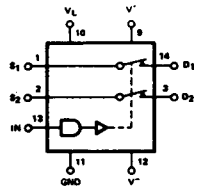


0157-21

DUAL SPDT
IH5143 ($r_{DS(on)}$ <75Ω)

SWITCH STATES ARE FOR LOGIC "1" INPUT

FLATPACK (FD-2)



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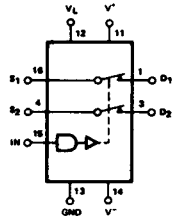
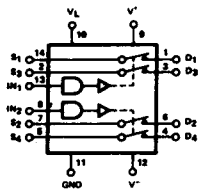
DIP (JE)



0157-23

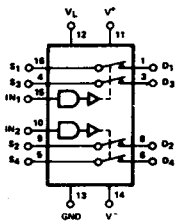
DPST
IH5144 ($r_{DS(on)}$ <75Ω)

FLATPACK (FD-2)



0157-25

DIP (JE) (DG185 EQUIVALENT)



0157-26

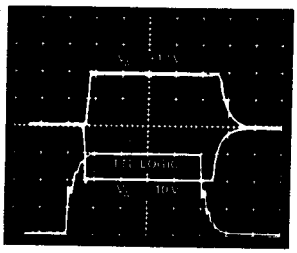
DUAL DPST
IH5145 ($r_{DS(on)}$ <75Ω)

Figure 6: Switching State Diagrams (Continued)

IH5140-IH5145 Family

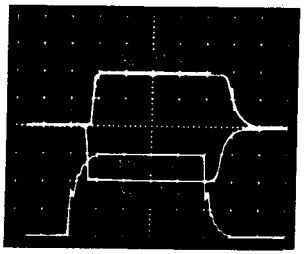
TYPICAL SWITCHING WAVEFORMS SCALE: VERT. = 5V/DIV. HORIZ. = 100ns/DIV.

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



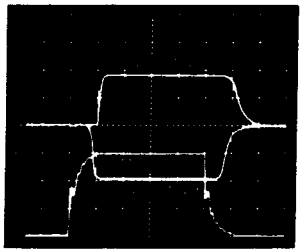
-55°C

0157-27



+25°C

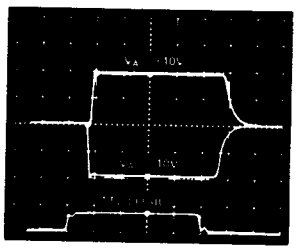
0157-28



+125°C

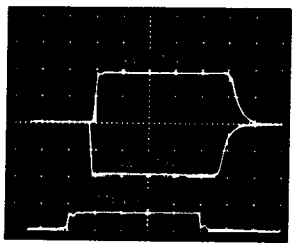
0157-29

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)



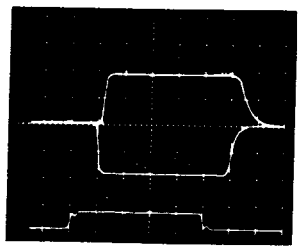
-55°C

0157-30



+25°C

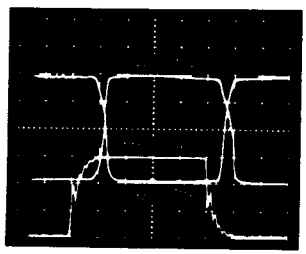
0157-31



+125°C

0157-32

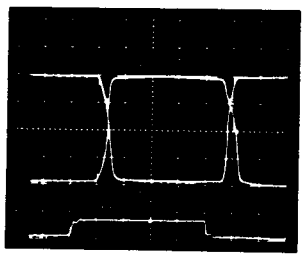
TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 10)



+25°C

0157-33

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 11)



+25°C

0157-34

APPLICATION NOTE

To maximize switching speed on the IH5140 family, TTL open collector logic (15V with a 1kΩ or less collector resistor) should be used. This configuration will result in (SPST) t_{on} and t_{off} times of 80ns and 50ns, for signals between −10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{on} is about 105ns, and t_{off} 75ns for SPST switches, and 135ns and 105ns (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V → +3.0V drive. Pin 13 is taken to −5V instead of the usual GND and strobe input is taken from +5V to −5V levels as shown in Figure 7.

The typical channel of the IH5140 family consists of both P and N-channel MOSFETs. The N-channel MOSFET uses a "Body Puller" FET to drive the body to −15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 8). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS}(ON)$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 9.

Current will flow from −10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 10. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

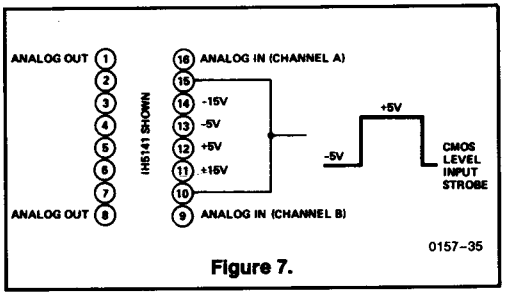


Figure 7.

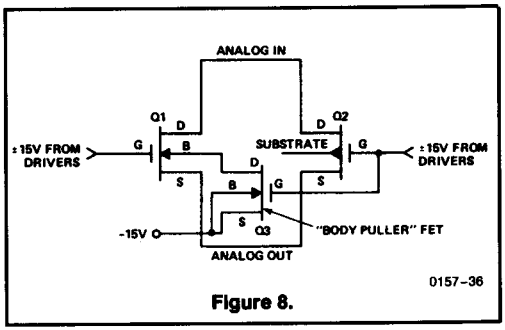


Figure 8.

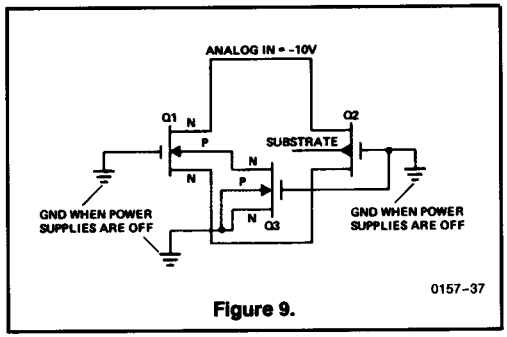


Figure 9.

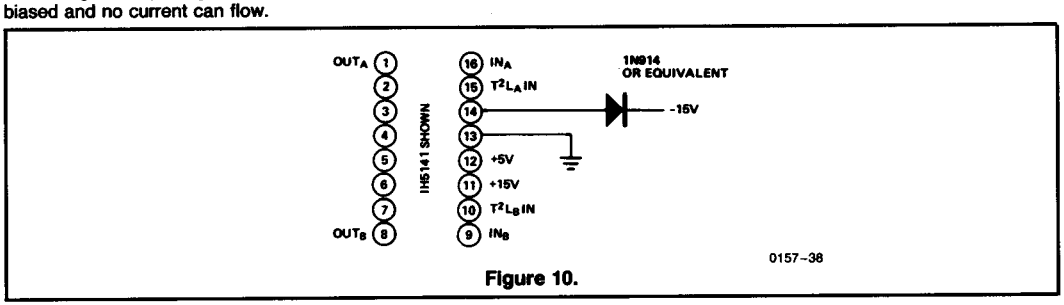


Figure 10.

IH5140-IH5145 Family

APPLICATIONS

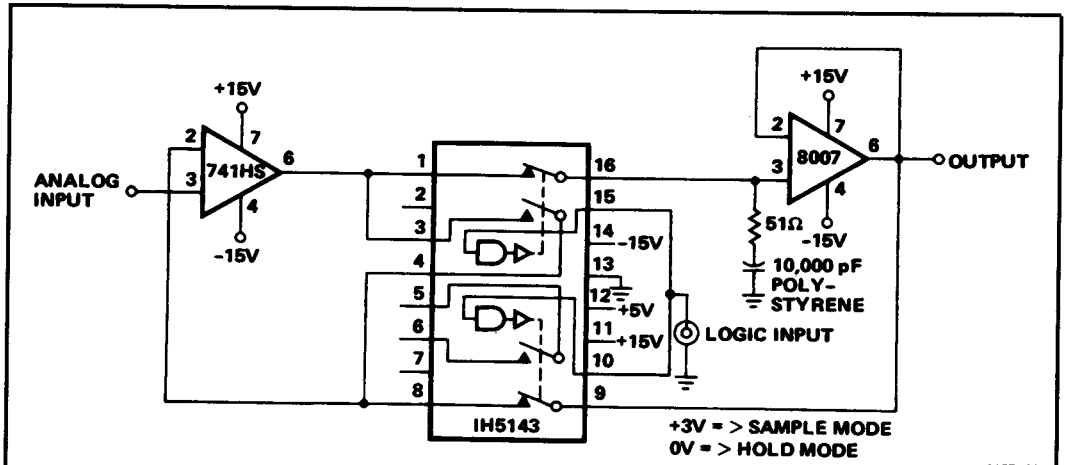
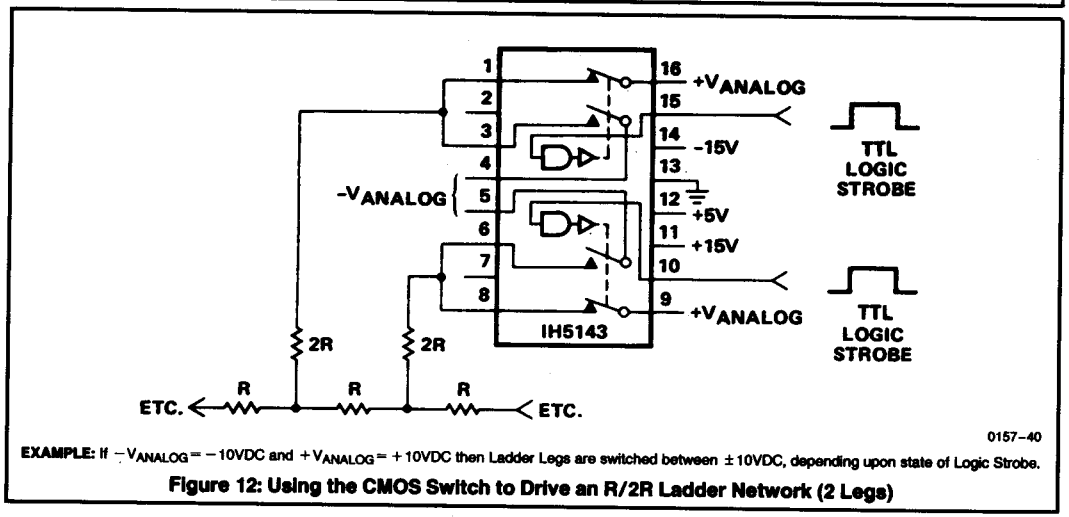


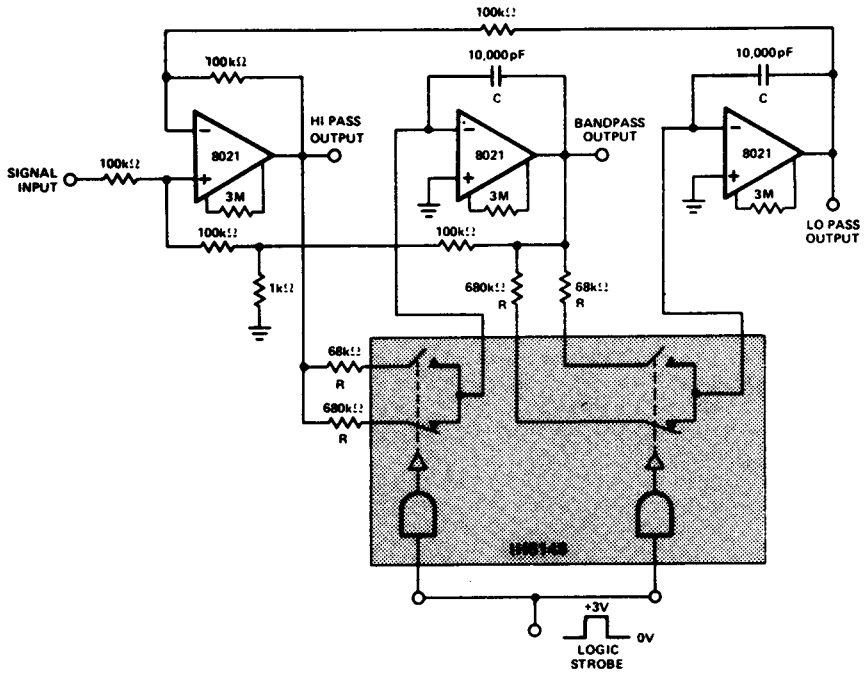
Figure 11: Improved Sample and Hold Using IH5143



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

Figure 12: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

APPLICATIONS (Continued)



0157-41

CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

Figure 13: Digitally Tuned Low Power Active Filter