

SCAN18245T

Non-Inverting Transceiver with TRI-STATE® Outputs

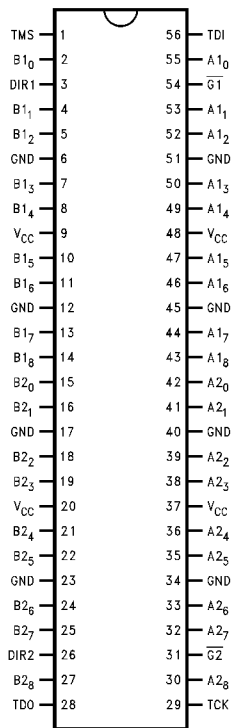
General Description

The SCAN18245T is a high speed, low-power bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Dual output enable control signals
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 24 mA/sink 48 mA
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch Cerpack package
- Includes CLAMP and HIGHZ instructions
- Available as Known Good Die
- Standard Microcircuit Drawing (SMD) 5962-9311501

Connection Diagram



DS100320-1

Pin Names	Description
B1 ₍₀₋₈₎	Side B1 Inputs or TRI-STATE Outputs
A2 ₍₀₋₈₎	Side A2 Inputs or TRI-STATE Outputs
B2 ₍₀₋₈₎	Side B2 Inputs or TRI-STATE Outputs
G1, G2	Output Enable Pins
DIR1, DIR2	Direction of Data Flow Pins

Pin Names	Description
A1 ₍₀₋₈₎	Side A1 Inputs or TRI-STATE Outputs

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SCAN18245T Non-Inverting Transceiver with TRI-STATE Outputs

Truth Tables

Inputs		A1 (0-8)	B1 (0-8)
$\overline{G1}$	DIR1		
L	L	H ←	H
L	L	L ←	L
L	H	H →	H
L	H	L →	L
H	X	Z	Z

Inputs		A2 (0-8)	B2 (0-8)
$\overline{G2}$	DIR2		
L	L	H ←	H
L	L	L ←	L
L	H	H →	H
L	H	L →	L
H	X	Z	Z

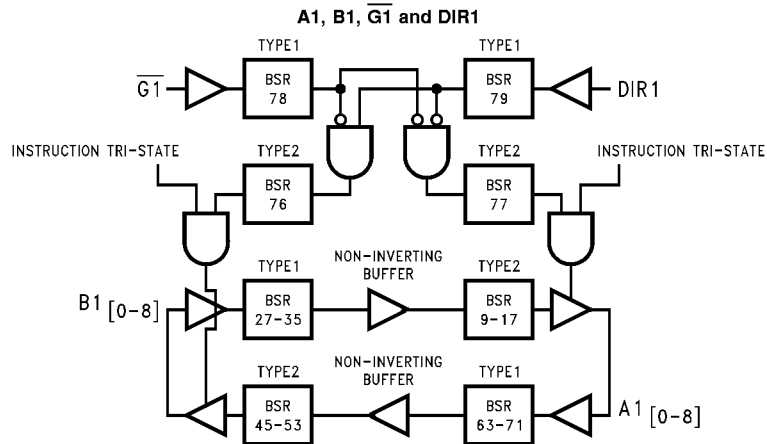
H= HIGH Voltage Level
 L= LOW Voltage Level
 X= Immaterial
 Z= High Impedance

Functional Description

The SCAN18245 consists of two sets of nine non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B ports to A ports, when HIGH en-

ables data from A ports to B ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B ports by placing them in a high impedance condition.

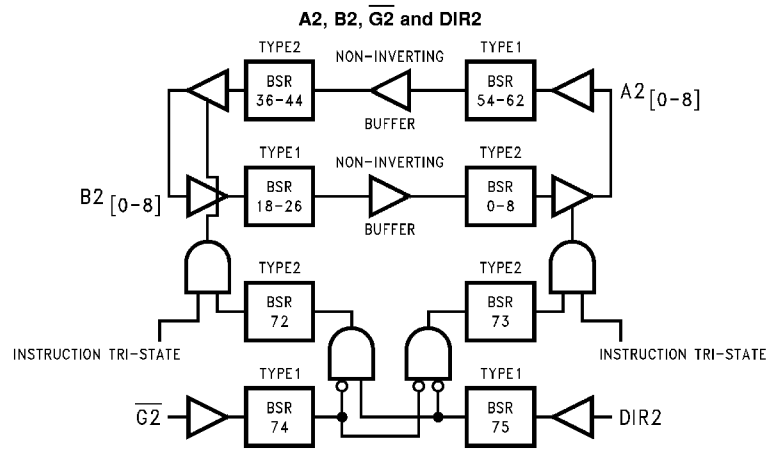
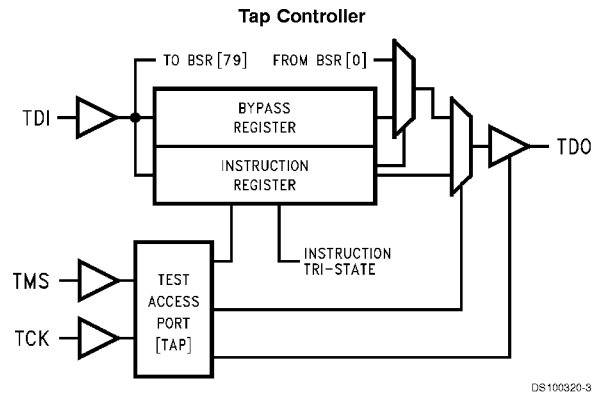
Block Diagrams



Note: BSR stands for Boundary Scan Register.

DS100320-2

Block Diagrams (Continued)



Note: BSR stands for Boundary Scan Register.

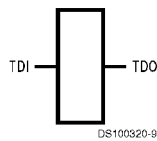
Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

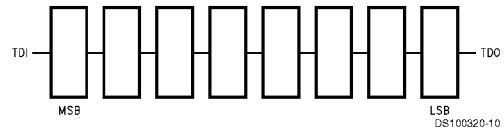
Bypass Register Scan Chain Definition Logic 0



The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18245T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition

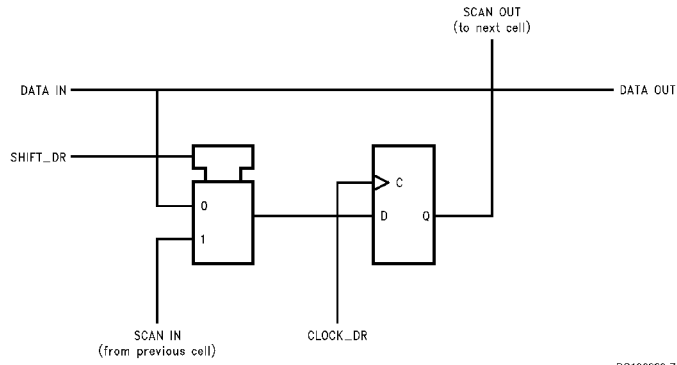


MSB → LSB

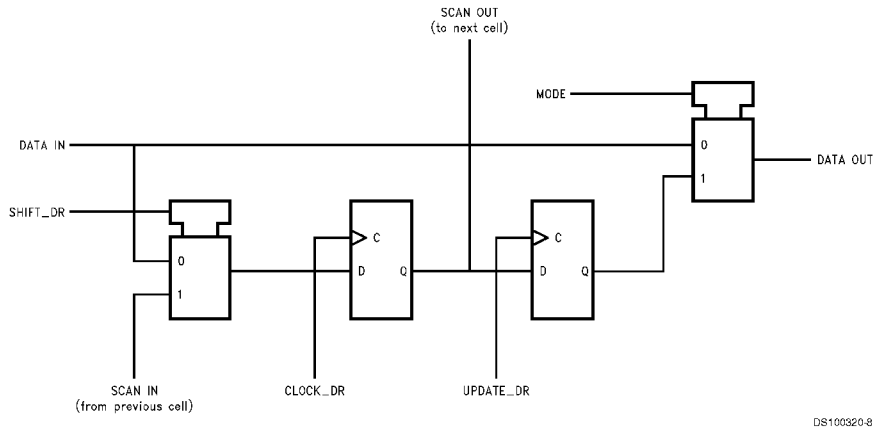
Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

Description of Boundary-Scan Circuitry (Continued)

Scan Cell TYPE1

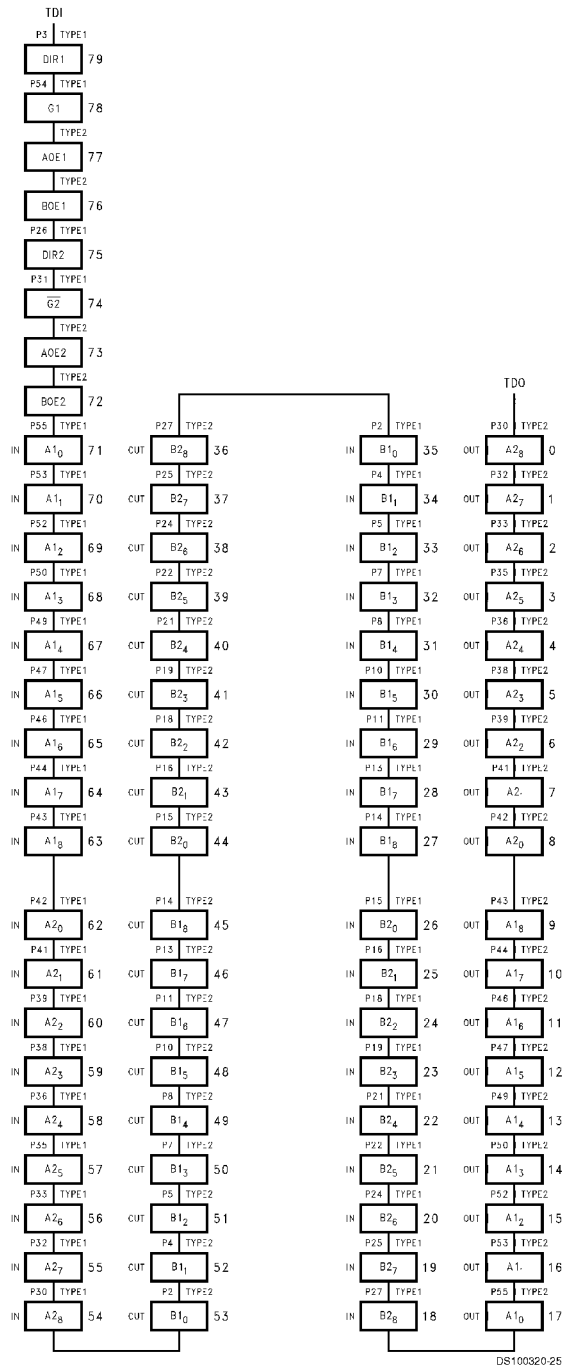


Scan Cell TYPE2



Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Scan Chain Definition (80 Bits in Length)



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Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	Control Signals
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE ₁		Internal	TYPE2	
76	BOE ₁		Internal	TYPE2	
75	DIR2	26	Input	TYPE1	
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE ₂		Internal	TYPE2	
72	BOE ₂		Internal	TYPE2	
71	A1 ₀	55	Input	TYPE1	A1-in
70	A1 ₁	53	Input	TYPE1	
69	A1 ₂	52	Input	TYPE1	
68	A1 ₃	50	Input	TYPE1	
67	A1 ₄	49	Input	TYPE1	
66	A1 ₅	47	Input	TYPE1	
65	A1 ₆	46	Input	TYPE1	
64	A1 ₇	44	Input	TYPE1	
63	A1 ₈	43	Input	TYPE1	
62	A2 ₀	42	Input	TYPE1	A2-in
61	A2 ₁	41	Input	TYPE1	
60	A2 ₂	39	Input	TYPE1	
59	A2 ₃	38	Input	TYPE1	
58	A2 ₄	36	Input	TYPE1	
57	A2 ₅	35	Input	TYPE1	
56	A2 ₆	33	Input	TYPE1	
55	A2 ₇	32	Input	TYPE1	
54	A2 ₈	30	Input	TYPE1	
53	B1 ₀	2	Output	TYPE2	B1-out
52	B1 ₁	4	Output	TYPE2	
51	B1 ₂	5	Output	TYPE2	
50	B1 ₃	7	Output	TYPE2	
49	B1 ₄	8	Output	TYPE2	
48	B1 ₅	10	Output	TYPE2	
47	B1 ₆	11	Output	TYPE2	
46	B1 ₇	13	Output	TYPE2	
45	B1 ₈	14	Output	TYPE2	
44	B2 ₀	15	Output	TYPE2	B2-out
43	B2 ₁	16	Output	TYPE2	
42	B2 ₂	18	Output	TYPE2	
41	B2 ₃	19	Output	TYPE2	
40	B2 ₄	21	Output	TYPE2	
39	B2 ₅	22	Output	TYPE2	
38	B2 ₆	24	Output	TYPE2	
37	B2 ₇	25	Output	TYPE2	
36	B2 ₈	27	Output	TYPE2	

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index (Continued)

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
35	B1 ₀	2	Input	TYPE1	B1-in
34	B1 ₁	4	Input	TYPE1	
33	B1 ₂	5	Input	TYPE1	
32	B1 ₃	7	Input	TYPE1	
31	B1 ₄	8	Input	TYPE1	
30	B1 ₅	10	Input	TYPE1	
29	B1 ₆	11	Input	TYPE1	
28	B1 ₇	13	Input	TYPE1	
27	B1 ₈	14	Input	TYPE1	
26	B2 ₀	15	Input	TYPE1	B2-in
25	B2 ₁	16	Input	TYPE1	
24	B2 ₂	18	Input	TYPE1	
23	B2 ₃	19	Input	TYPE1	
22	B2 ₄	21	Input	TYPE1	
21	B2 ₅	22	Input	TYPE1	
20	B2 ₆	24	Input	TYPE1	
19	B2 ₇	25	Input	TYPE1	
18	B2 ₈	27	Input	TYPE1	
17	A1 ₀	55	Output	TYPE2	A1-out
16	A1 ₁	53	Output	TYPE2	
15	A1 ₂	52	Output	TYPE2	
14	A1 ₃	50	Output	TYPE2	
13	A1 ₄	49	Output	TYPE2	
12	A1 ₅	47	Output	TYPE2	
11	A1 ₆	46	Output	TYPE2	
10	A1 ₇	44	Output	TYPE2	
9	A1 ₈	43	Output	TYPE2	
8	A2 ₀	42	Output	TYPE2	A2-out
7	A2 ₁	41	Output	TYPE2	
6	A2 ₂	39	Output	TYPE2	
5	A2 ₃	38	Output	TYPE2	
4	A2 ₄	36	Output	TYPE2	
3	A2 ₅	35	Output	TYPE2	
2	A2 ₆	33	Output	TYPE2	
1	A2 ₇	32	Output	TYPE2	
0	A2 ₈	30	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current (I_O)	± 70 mA
DC V_{CC} or Ground Current	
Per Output Pin	± 70 mA
Junction Temperature	
Cerpack	+175°C
Storage Temperature	-65°C to +150°C

ESD (Min)

2000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Military	-55°C to +125°C
Minimum Input Edge Rate dV/dt	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Military	Units	Conditions
			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			Guaranteed Limits		
V_{IH}	Minimum High Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
V_{OH}	Minimum High Output Voltage	4.5	3.15	V	$I_{OUT} = -50 \mu A$
		5.5	4.15		
		4.5	2.4	V	
		5.5	2.4		
V_{OL}	Maximum Low Output Voltage	4.5	0.1	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.55	V	
		5.5	0.55		
I_{IN}	Maximum Input Leakage Current	5.5	± 1.0	μA	$V_I = V_{CC}, \text{GND}$
I_{IN} TDI, TMS	Maximum Input Leakage	5.5	3.7	μA	$V_I = V_{CC}$
			-385	μA	$V_I = \text{GND}$
			-160	μA	$V_I = \text{GND}$
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5	63	mA	$V_{OLD} = 0.8V \text{ Max}$
I_{OHD}			-27	mA	$V_{OHD} = 2.0V \text{ Min}$
I_{OZT}	Maximum I/O Leakage Current	5.5	± 11.0	μA	$V_I (\text{OE}) = V_{IL}, V_{IH}$ $V_I = V_{CC}, \text{GND}$ $V_O = V_{CC}, \text{GND}$
I_{OS}	Output Short Circuit Current	5.5	-100	mA (min)	$V_O = 0V$
I_{CC}	Maximum Quiescent Supply Current	5.5	168	μA	$V_O = \text{High}$ TDI, TMS = V_{CC}
		5.5	930	μA	$V_O = \text{High}$ TDI, TMS = GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	Military		Units	Conditions
			T _A = -55°C to +125°C			
			Guaranteed Limits			
I _{CC1}	Maximum I _{CC} Per Input	5.5	2.0		mA	V _I = V _{CC} -2.1V
		5.5	2.15		mA	V _I = V _{CC} -2.1V TDI/TMS Pin, test one with the other floating

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications

Symbol	Parameter	V _{CC} (V)	Military		Units
			T _A = -55°C to +125°C		
			Guaranteed Limits		
V _{OLP}	Maximum High Output Noise (Notes 4, 5)	5.0	0.8		V
V _{OLV}	Minimum Low Output Noise (Notes 4, 5)	5.0	-0.8		V

Note 4: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

AC Electrical Characteristics

Normal Operation

Symbol	Parameter	V _{CC} (V) (Note 7)	Military		Units
			T _A = -55°C to +125°C		
			C _L = 50 pF		
			Min	Max	
t _{PLH}	Propagation Delay A to B, B to A	5.0	1.6	10.0	ns
t _{PHL}			1.6	11.0	
t _{PLZ}	Disable Time	5.0	1.2	10.0	ns
t _{PHZ}			1.2	9.5	
t _{PZL}	Enable Time	5.0	1.6	13.0	ns
t _{PZH}			1.6	11.0	

AC Electrical Characteristics

Scan Test Operation

Symbol	Parameter	V _{CC} (V) (Note 7)	Military		Units
			T _A = -55° C to +125° C C _L = 50 pF		
			Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay TCK to TDO	5.0	2.8	15.8	ns
t _{PLZ} , t _{PHZ}	Disable Time TCK to TDO	5.0	2.0	12.8	ns
t _{PZL} , t _{PZH}	Enable Time TCK to TDO	5.0	2.4	16.7	ns
t _{PLH} , t _{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0	21.7	ns
t _{PLH} , t _{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	4.0	21.2	ns
t _{PLH} , t _{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	4.4	23.0	ns
t _{PLZ} , t _{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	3.2	19.6	ns
t _{PLZ} , t _{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	2.8	20.9	ns
t _{PLZ} , t _{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	2.8	21.8	ns
t _{PZL} , t _{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0	22.6	ns
t _{PZL} , t _{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	3.2	23.7	ns
t _{PZL} , t _{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	3.6	24.9	ns

Note 6: All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements

Scan Test Operation

Symbol	Parameter	V _{CC} (V) (Note 7)	Military	Units	
			T _A = -55°C to +125°C C _L = 50 pF		
			Guaranteed Minimum		
t _S	Setup Time, H or L Data to TCK (Note 8)	5.0	0.0	ns	
t _H	Hold Time, H or L TCK to Data (Note 8)	5.0	6.5	ns	
t _S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK (Note 9)	5.0	0.0	ns	
t _H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$ (Note 9)	5.0	4.0	ns	
t _S	Setup Time, H or L DIR1, DIR2 to TCK (Note 11)	5.0	0.0	ns	
t _H	Hold Time, H or L TCK to DIR1, DIR2 (Note 11)	5.0	4.0	ns	
t _S	Setup Time, H or L Internal AOE _n , BOE _n to TCK (Note 10)	5.0	1.0	ns	
t _H	Hold Time, H or L TCK to Internal AOE _n , BOE _n (Note 10)	5.0	4.0	ns	
t _S	Setup Time, H or L TMS to TCK	5.0	7.0	ns	
t _H	Hold Time, H or L TCK to TMS	5.0	2.0	ns	
t _S	Setup Time, H or L TDI to TCK	5.0	1.0	ns	
t _H	Hold Time, H or L TCK to TDI	5.0	3.5	ns	
t _W	Pulse Width	5.0	H	12.0	ns
			L	5.0	
f _{max}	Maximum TCK Clock Frequency	5.0	25	MHz	
T _{PU}	Wait Time, Power Up to TCK	5.0	100	ns	
T _{DN}	Power Down Delay	0.0	100	ms	

Note 7: Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 8: Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0–8, 9–17, 18–26, 27–35, 36–44, 45–53, 54–62, 63–71).

Note 9: Timing pertains to BSR 74 and 78 only.

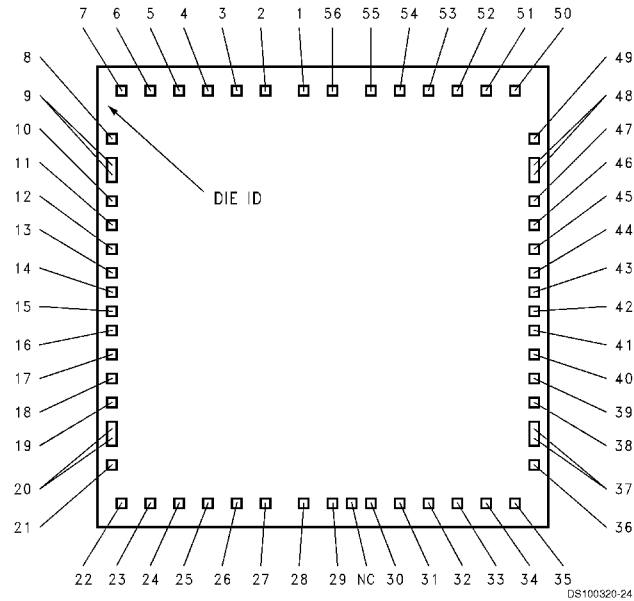
Note 10: Timing pertains to BSR 72, 73, 76 and 77 only.

Note 11: Timing pertains to BSR 75 and 79 only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	20	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	41	pF	$V_{CC} = 5.0V$

Pad Diagram



SCAN18245T Die Information

Die Revision	Z
Die ID	Y8J245
Die Size (X)	4310 μm
Die Size (Y)	4310 μm
Die Thickness	14 mil
Substrate Bias	V _{CC} (optional)
Backside Coating	None

Pad Locations

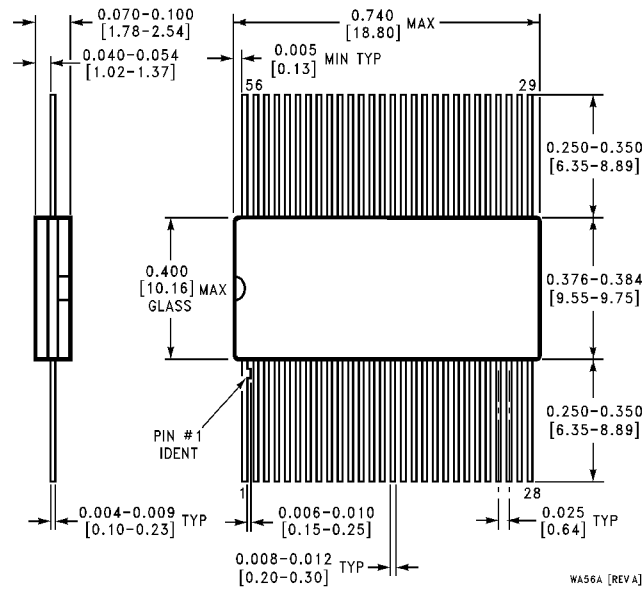
Signal Number	Signal Name	Pad Location (Note 12)
1	TMS	-8.58, 77.81
2	B1 ₀	-19.94, 77.81
3	DIR1	-30.50, 77.81
4	B1 ₁	-40.98, 77.81
5	B1 ₂	-53.59, 77.81
6	GND	-63.73, 77.81
7	B1 ₃	-74.47, 77.81
8	B1 ₄	-79.73, 62.30
9	V _{CC}	-79.73, 51.55
		-79.73, 46.28
10	B1 ₅	-79.73, 36.05
11	B1 ₆	-79.73, 27.48
12	GND	-79.72, 19.46
13	B1 ₇	-79.73, 10.09
14	B1 ₈	-79.73, 3.46
15	B2 ₀	-79.73, -3.43
16	B2 ₁	-79.73, -10.06
17	GND	-79.72, -19.43
18	B2 ₂	-79.73, -27.45
19	B2 ₃	-79.73, -36.02
20	V _{CC}	-79.73, -46.24
		-79.73, -51.52
21	B2 ₄	-79.73, -62.27
22	B2 ₅	-74.47, -77.81
23	GND	-63.73, -77.81
24	B2 ₆	-53.59, -77.81
25	B2 ₇	-40.98, -77.81
26	DIR2	-30.50, -77.81
27	B2 ₈	-19.94, -77.81
28	TDO	-8.58, -77.81
29	TCK	5.54, -77.81
30	A2 ₈	19.94, -77.81
31	$\overline{\text{G2}}$	30.50, -77.81
32	A2 ₇	40.98, -77.81
33	A2 ₆	53.59, -77.81
34	GND	63.73, -77.81
35	A2 ₅	74.47, -77.81
36	A2 ₄	79.73, -62.27

Pad Locations (Continued)

Signal Number	Signal Name	Pad Location (Note 12)
37	V _{CC}	79.73, -51.50
		79.73, -46.23
38	A2 ₃	79.73, -36.02
39	A2 ₂	79.73, -27.40
40	GND	79.73, -19.43
41	A2 ₁	79.73, -10.06
42	A2 ₀	79.73, -3.43
43	A1 ₈	79.73, 3.46
44	A1 ₇	79.73, 10.09
45	GND	79.72, 19.46
46	A1 ₆	79.73, 27.43
47	A1 ₅	79.73, 36.05
48	V _{CC}	79.73, 46.26
		79.73, 51.54
49	A1 ₄	79.73, 62.30
50	A1 ₃	74.47, 77.81
51	GND	63.73, 77.81
52	A1 ₂	53.59, 77.81
53	A1 ₁	40.98, 77.81
54	G1	30.50, 77.81
55	A1 ₀	19.94, 77.81
56	TDI	5.54, 77.81

Note 12: X, Y coordinates measured in mils from center of die.

Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Ceramic Flatpak (F)
 NS Package Number WA56A**

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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