8T10
Bus Flip-Flop

3-State Quad D-Type Bus Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A master reset input resets all flip-flops upon application of a logic "1" level.

Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T10	24ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N8T10N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
D_n, CP	Input	1ul
E_n, MR, $0E_n$	Input	1.2ul
Q_n	Output	10ul

NOTE:
A unit load (ul) is 40μA I_{IH} and −1.6mA I_{IL}.

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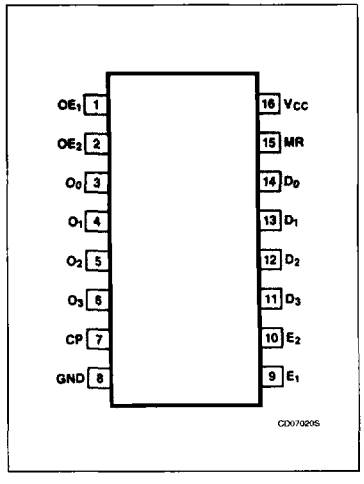
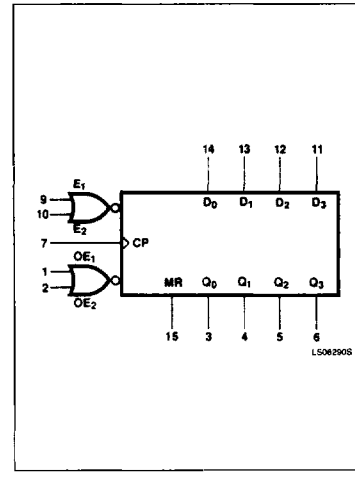
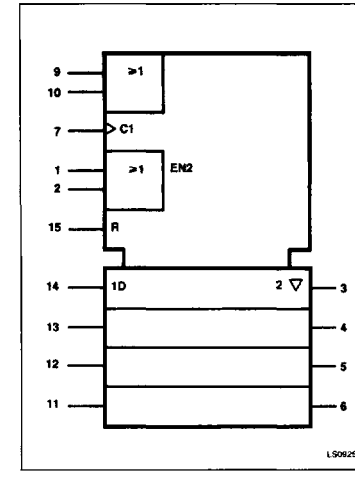
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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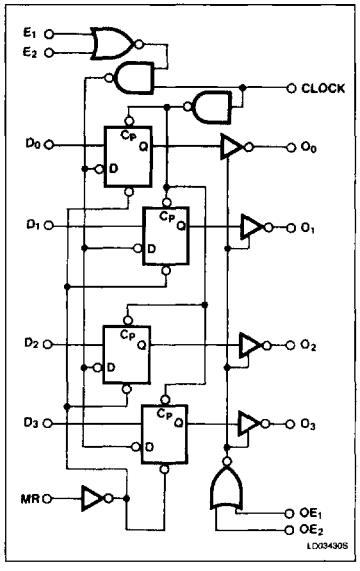
LOGIC DIAGRAM



FUNCTION TABLE

D_n	E	OE	Q_{n+1}
0	0	0	0
1	0	0	1
X	1	0	Q_n
X	X	1	High Z

NOTES:
1. Q_n refers to the output state before a clock pulse.
2. $Q_n + 1$ refers to the output state after a clock pulse.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−12	mA
I_{OH}	HIGH-level output current			−5.2	mA
I_{OL}	LOW-level output current			32	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		8T10 Min	8T10 Max	UNIT
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −12mA			−1.5	V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, I_{OH} = −5.2mA		2.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, I_{OL} = 32mA			0.4	V
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 4.5V	Dn		40	μA
			Cp		40	μA
			Others		50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	Dn		−3.2	mA
			Cp		−3.2	mA
			Others		−2.0	mA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX		−40	−120	mA
I_{CC}	Supply current (total)	V_{CC} = 5.25V			118	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS		8T Min	8T Max	UNIT
t_{MAX}	Maximum clock frequency	Figure 1		35		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Figure 1	C_L = 30pF		25	ns
			C_L = 300pF		35	
t_{PHL}	Propagation delay, MR to output	Figure 2	C_L = 30pF		22	ns
			C_L = 300pF		30	
t_{PZH}	Output enable to HIGH level					ns
t_{PZL}	Output enable to LOW level	Figure 4	C_L = 300pF		30	ns
t_{PHZ}	Output disable from HIGH level					ns
t_{PLZ}	Output disable from LOW level	Figure 4	C_L = 300pF		30	ns

NOTE:
For industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8T10 Min	8T10 Max	UNIT
t_W(CP)	Clock pulse width	Figure 1		12	ns
t_W(MR)	MR pulse width	Figure 2	15		ns
t_s	Set-up time, data to clock	Figure 1	5		ns
t_h	Hold time, data to clock	Figure 3		5	ns

AC TEST CIRCUITS AND WAVEFORMS

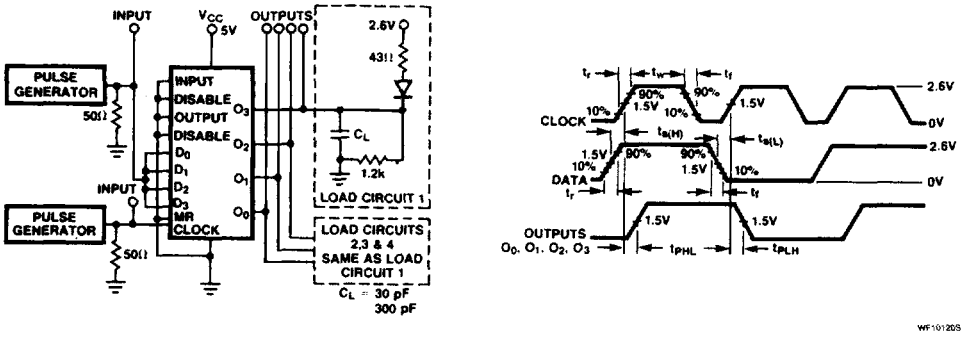


Figure 1. Propagation Delay t_{PHL} t_{PLH} (Clock To Output)

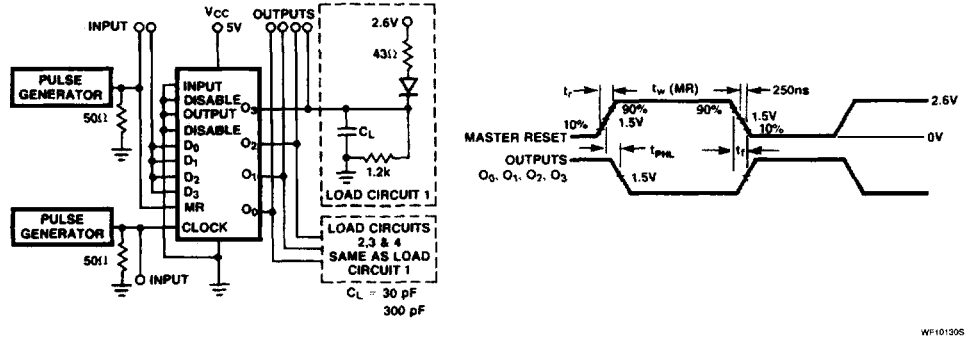


Figure 2. Propagation Delay t_{PHL} (Master Reset To Output)

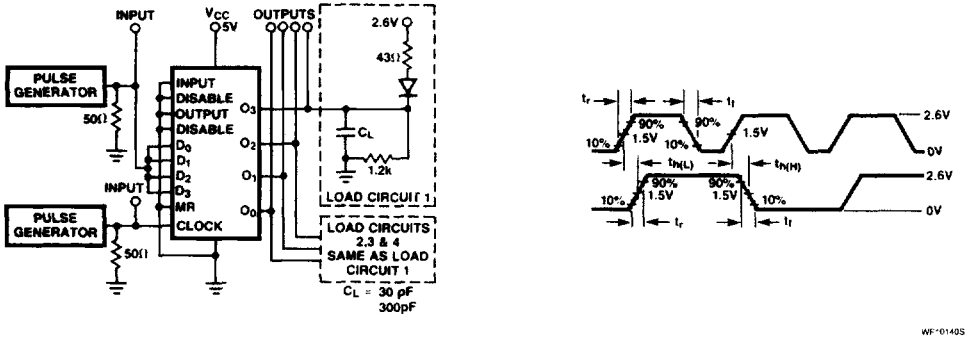


Figure 3. Propagation Delay (Data Hold Time)

AC TEST CIRCUITS AND WAVEFORMS (Continued)

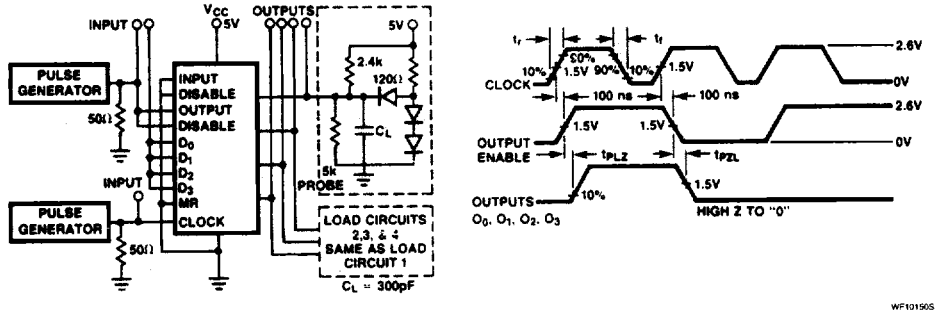
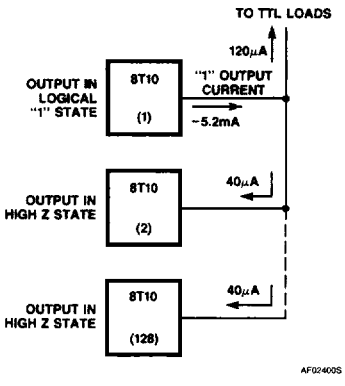
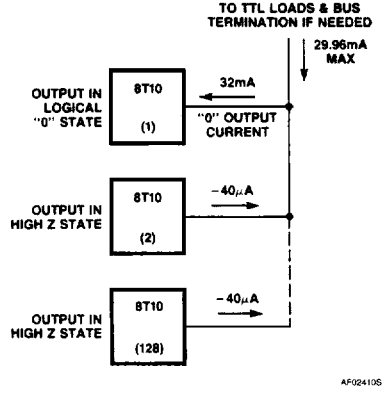


Figure 4. Propagation Delay (Enable To Output)

TYPICAL APPLICATIONS



Driver In Logical "1" State



Driver In Logical "0" State

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