ABT and MULTIBYTE FAMILY SPECIFICATIONS

General

These family specifications cover the common electrical ratings and characteristics of the entire 74ABT and MULTIBYTE families, unless otherwise specified in the individual device data sheet.

Introduction

The ABT, ABT16 and MULTIBYTE™ Advanced BiCMOS (QUBiC) families combine the low power dissipation and low noise of BiCMOS with the high output drive of our bipolar logic devices. The basic families of devices designated as 74ABTxxx/74ABT16xxx and MBxxxx will operate at BiCMOS input logic levels for high noise immunity, negligible quiescent supply and input current. They operate from a power supply of 4.5 to 5.5 V.

Handling BiCMOS devices

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take appropriate handling precautions into account.

ABT features

- Fastest in industry apart from ECL devices
- Ideal for bus driver applications
- Very short propagation delays
- 64 mA sink current; 32 mA source current
- Supply voltage range: 5 V ±10%
- Standard TTL pin-out
- Latch-up protection exceeds 500 mA
- Wide operating temperature range: −40 to +85 °C
- Devices available in DIL and SO and SSOP packages
- Live insertion/extraction permitted

MULTIBYTE features

- Double-byte functionality
- TTL compatible I/Os
- 50 µA I_{CCZ}
- +64/−32 mA output drive
- High performance, JEDEC registered 52-pin package
- Very low noise immunity
- Very low simultaneous switching propagation delay degradation
- Very low skew

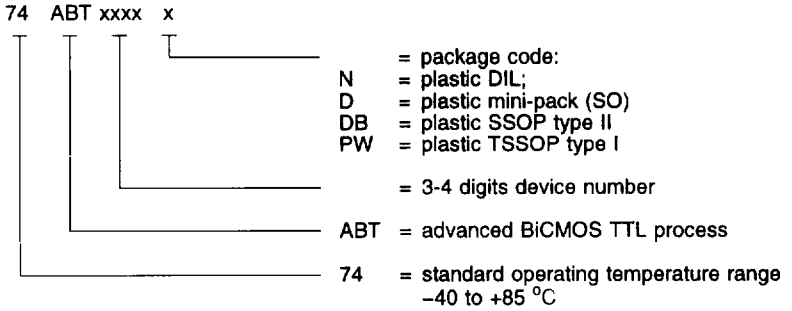
ABT16 features

- Multiple-byte functionality
- Multiple Vcc and GND pins minimize switching noise
- 64 mA sink current; 32 mA source current
- Devices available in SSOP and TSSOP packages
- Live insertion/extraction permitted
- BVS hold circuit on data inputs

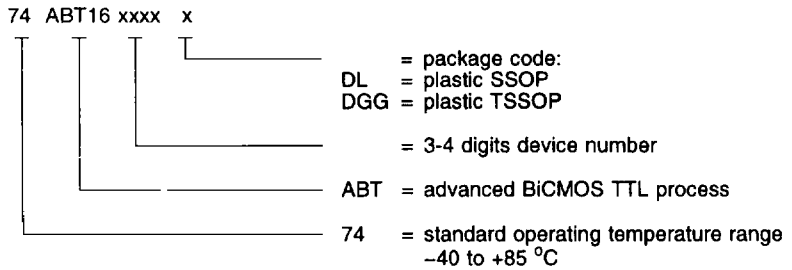
Type number designation

Basic family:

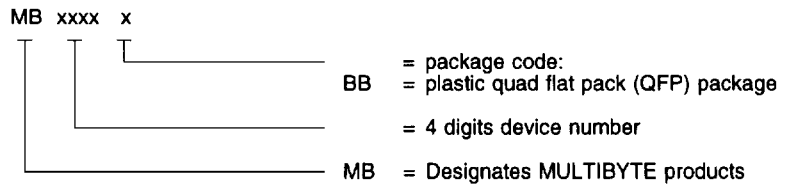
74ABTxxxx



74ABT16xxxx



MBxxxxx



Family ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

parameter	conditions	symbol	min.	max.	unit
DC supply voltage		V_{CC}	−0.5	+7	V
DC input diode current	$V_I < 0$ V	$-I_{IK}$	–	18	mA
DC input voltage		V_I	−1.2	+7	V
DC output diode current	$V_O < 0$ V	$-I_{OK}$	–	50	mA
DC output voltage	output OFF or HIGH	V_O	−0.5	+5.5	V
DC output current	output LOW	I_O	–	128	mA
storage temperature range		T_{stg}	−65	+150	°C

Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

parameter	symbol	min.	max.	unit
DC supply voltage	V_{CC}	4.5	5.5	V
Input voltage	V_I	0	V_{CC}	V
HIGH level input voltage	V_{IH}	2.0	–	V
LOW level input voltage	V_{IL}	–	0.8	V
HIGH level output current	I_{OH}	–	32	mA
LOW level output current	I_{OL}	–	64	mA
Input transition rise or fall rate	$\Delta t/\Delta V$	0	5	ns/V
Operating ambient temperature range	T_{amb}	−40	+85	°C

ABT DC family characteristics

Voltages are referenced to GND (ground = 0 V)

parameter	V_{CC} (V)	symbol	T_{amb} (°C) +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	unit	conditions V_I	conditions other
Input clamp voltage	4.5	V_{IK}	–	−0.9	−1.2	–	−1.2	V		I_{IK} = −18 mA
HIGH level output voltage	4.5	V_{OH}	2.5	2.9	–	2.5	–	V	V_{IH} or V_{IL}	I_O = −3 mA
	5.0		3.0	3.4	–	3.0	–	V		I_O = −3 mA
	4.5		2.0	2.4	–	2.0	–	V		I_O = −32 mA
LOW level output voltage	4.5	V_{OL}	–	0.42	0.55	–	0.55	V	V_{IH} or V_{IL}	I_{OL} = 64 mA
Power-up LOW voltage[3]	5.5	V_{RST}	–	0.13	0.55	–	0.55	V	5.5 V or 0 V	I_O = 1 mA
Input leakage current	5.5	I_I	–	±0.01	±0.1	–	±0.1	µA	GND or 5.5 V	
Power-off leakage current	0.0	I_{OFF}	–	±5.0	±100	–	±100	µA		V_O or V_I ≤4.5 V
Power up/down 3-state output current[4]	2.1	$I_{PU/PD}$	–	±5.0	±50	–	±50	µA	V_{CC} or GND	V_{OE} = don't cace
3-state output HIGH current	5.5	I_{OZH}	–	5.0	50	–	50	µA	V_{IH} or V_{IL}	V_O = 2.7 V
3-state output LOW current	5.5	I_{OZL}	–	−5.0	−50	–	−50	µA	V_{IH} or V_{IL}	V_O = 0.5 V
Output HIGH leakage current	5.5	I_{CEX}	–	5.0	50	–	50	µA	V_{CC} or GND	V_O = 2.5 V
Output HIGH current[1]	5.5	I_O	−50	−65	−180	−50	−180	mA		V_O = 2.5 V
Quiescent supply current	5.5	I_{CCH}	–	120	250	–	250	µA	V_{CC} or GND	outputs HIGH
	5.5	I_{CCL}	–	24	30	–	30	mA		outputs LOW
	5.5	I_{CCZ}	–	120	250	–	250	µA		outputs 3-state
Additional supply current per input pin[2]	5.5	ΔI_{CC}	–	0.5	1.5	–	1.5	mA	V_{CC} or GND	outputs 3-state; one input at 3.4 V

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ±10%, a transition time of up to 100 µs is permitted. This note applies only to parts with the live insertion/extraction feature.

ABT16 DC family characteristics

Voltages are referenced to GND (ground = 0 V)

parameter	V_{CC} (V)	symbol	T_{amb} (°C) +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	unit	conditions V_I	conditions other
Input clamp voltage	4.5	V_{IK}	–	−0.9	−1.2	–	−1.2	V		I_{IK} = −18 mA
HIGH level output voltage	4.5	V_{OH}	2.5	2.9	–	2.5	–	V	V_{IH} or V_{IL}	I_O = −3 mA
	5.0		3.0	3.4	–	3.0	–	V		I_O = −3 mA
	4.5		2.0	2.4	–	2.0	–	V		I_O = −32 mA
LOW level output voltage	4.5	V_{OL}	–	0.42	0.55	–	0.55	V	V_{IH} or V_{IL}	I_{OL} = 64 mA
Power-up LOW voltage[3]	5.5	V_{RST}	–	0.13	0.55	–	0.55	V	5.5 V or 0 V	I_O = 1 mA
Input leakage current	5.5	I_I	–	±0.01	±0.1	–	±0.1	µA	GND or 5.5 V	
Power-off leakage current	0.0	I_{OFF}	–	±5.0	±100	–	±100	µA		V_O or V_I ≤4.5 V
Power up/down 3-state output current[4]	2.1	$I_{PU/PD}$	–	±5.0	±50	–	±50	µA	V_{CC} or GND	V_{OE} = don't cace
3-state output HIGH current	5.5	I_{OZH}	–	5.0	50	–	50	µA	V_{IH} or V_{IL}	V_O = 2.7 V
3-state output LOW current	5.5	I_{OZL}	–	−5.0	−50	–	−50	µA	V_{IH} or V_{IL}	V_O = 0.5 V
Output HIGH leakage current	5.5	I_{CEX}	–	5.0	50	–	50	µA	V_{CC} or GND	V_O = 2.5 V
Output HIGH current[1]	5.5	I_O	−50	–	−200	−50	−200	mA		V_O = 2.5 V
Quiescent supply current	5.5	I_{CCH}	–	–	2	–	2	mA	V_{CC} or GND	outputs HIGH
	5.5	I_{CCL}	–	–	41	–	41	mA		outputs LOW
	5.5	I_{CCZ}	–	–	2	–	2	mA		outputs 3-state
Additional supply current per input pin[2]	5.5	ΔI_{CC}	–	–	1.5	–	1.5	mA	V_{CC} or GND	outputs 3-state; one input at 3.4 V

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ±10%, a transition time of up to 100 µs is permitted. This note applies only to parts with the live insertion/extraction feature.

MULTIBYTE DC family characteristics

Voltages are referenced to GND (ground = 0 V)

parameter	V_{CC} (V)	symbol	T_{amb} (°C) +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	unit	conditions V_I	conditions other
Input clamp voltage	4.5	V_{IK}	–	−0.9	−1.2	–	−1.2	V		I_{IK} = −18 mA
HIGH level output voltage	4.5 5.0 4.5	V_{OH}	2.5 3.0 2.0	2.9 3.4 2.4	– – –	2.5 3.0 2.0	– – –	V V V	V_{IH} or V_{IL}	I_O = −3 mA I_O = −3 mA I_O = −32 mA
LOW level output voltage	4.5	V_{OL}	–	0.42	0.55	–	0.55	V	V_{IH} or V_{IL}	I_{OL} = 64 mA
Power-up LOW voltage[3]	5.5	V_{RST}	–	0.13	0.55	–	0.55	V	5.5 V or 0 V	I_O = 1 mA
Input leakage current	5.5	I_I	–	±0.01	±0.1	–	±0.1	µA	GND or 5.5 V	
Power-off leakage current	0.0	I_{OFF}	–	±5.0	±100	–	±100	µA		V_O or V_I ≤4.5 V
Power up/down 3-state output current[4]	2.1	$I_{PU/PD}$	–	±5.0	±50	–	±50	µA	V_{CC} or GND	V_{OE} = don't cace
3-state output HIGH current	5.5	I_{OZH}	–	5.0	50	–	50	µA	V_{IH} or V_{IL}	V_O = 2.7 V
3-state output LOW current	5.5	I_{OZL}	–	−5.0	−50	–	−50	µA	V_{IH} or V_{IL}	V_O = 0.5 V
Output HIGH leakage current	5.5	I_{CEX}	–	5.0	50	–	50	µA	V_{CC} or GND	V_O = 2.5 V
Output HIGH current[1]	5.5	I_O	−50	–	−180	−50	−180	mA		V_O = 2.5 V
Quiescent supply current	5.5 5.5 5.5	I_{CCH} I_{CCL} I_{CCZ}	– – –	– – –	250 60 250	– – –	250 60 250	µA mA µA	V_{CC} or GND	outputs HIGH outputs LOW outputs 3-state
Additional supply current per input pin[2]	5.5	ΔI_{CC}	–	0.5	1.5	–	1.5	mA	V_{CC} or GND	outputs 3-state; one input at 3.4 V

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ±10%, a transition time of up to 100 µs is permitted. This note applies only to parts with the live insertion/extraction feature.

ABT/ABT16 & MULTIBYTE SERIES		ABT	ABT16	MB
GATES				
00	Quad 2-input NAND gate	○		
02	Quad 2-input NOR gate	○		
04	Hex inverter	○		
08	Quad 2-input AND gate	○		
10	Triple 3-input NAND gate	○		
20	Dual 4-input NAND gate	○		
32	Quad 2-input OR gate	○		
BUFFERS/LINE DRIVERS				
125	Quad buffer; 3-state	○		
126	Quad buffer; 3-state	○		
240	Octal inverting buffer; 3-state	○		
240	16-bit inverting buffer; 3-state		○	
240-1	Octal inverting buffer with 30 Ω termination resistors; 3-state	○		
240-1	16-bit inverting buffer; 3-state		○	
241	Octal buffer/line driver; 3-state	○		
241	16-bit buffer/line driver; 3-state		○	
244	Octal buffer/line driver; 3-state	○		
244A	16-bit buffer/line driver; 3-state		○	
244-1	Octal buffer/line driver with 30 Ω termination resistors; 3-state	○		
244-1	16-bit buffer/line driver with 30 Ω termination resistors; 3-state		○	
540	Octal buffer; inverting; 3-state	○		
541	Octal buffer/line driver; 3-state	○		
827	10-bit buffer/line driver; non-inverting; 3-state	○		
827A	20-bit buffer/line driver; non-inverting; 3-state		○	
2240	Octal inverting buffer with 30 Ω termination resistors; 3-state	○		
2240	16-bit inverting buffer; 3-state		○	○
2241	16-bit buffer/line driver; 3-state			○
2244	Octal buffer/line driver with 30 Ω termination resistors; 3-state	○		
2244	16-bit buffer/line driver with 30 Ω termination resistors; 3-state		○	
2244	16-bit buffer/line driver; 3-state			○
2541	16-bit buffer/line driver; 3-state			○
2827	20-bit buffer/line driver; non-inverting; 3-state			○
D-type FLIP-FLOPS/LATCHES				
74	Dual D-type edge triggered flip-flop	○		
273	16-bit D flip-flop		○	
273A	Octal D flip-flop	○		
273A	16-bit D flip-flop		○	
373A	Octal D-type transparent latch; 3-state	○		
373B	16-bit D-type transparent latch; 3-state		○	
374A	Octal D-type flip-flop; positive-edge trigger; 3-state	○		
374B	16-bit D-type flip-flop; positive-edge trigger; 3-state		○	
377	Octal D-type flip-flop with enable	○		
534	Octal D-type flip-flop; inverting; 3-state	○		
573A	Octal D-type transparent latch; 3-state	○		
574A	Octal D-type flip-flop; 3-state	○		
821	10-bit D-type flip-flop; positive-edge trigger; 3-state	○		
821A	20-bit D-type flip-flop; positive-edge trigger; 3-state		○	
823	9-bit D-type flip-flop with reset and enable; 3-state	○		
823A	18-bit D-type flip-flop with reset and enable; 3-state		○	
825A	16-bit bus interface register; non-inverting; 3-state		○	
841	10-bit bus interface latch; 3-state	○		
841A	20-bit bus interface latch; 3-state		○	
843	9-bit bus interface latch with set and reset; 3-state	○		
845	8-bit bus interface latch with set and reset; 3-state	○		
2373	16-bit D-type transparent latch; 3-state			○
2374	16-bit D-type flip-flop; positive-edge trigger; 3-state			○
2377	16-bit D-type flip-flop with enable			○

ABT/ABT16 & MULTIBYTE SERIES		ABT	ABT16	MB
2821	20-bit D-type flip-flop; positive-edge trigger; 3-state			
2823	18-bit D-type flip-flop with reset and enable; 3-state			
2841	20-bit bus interface latch; 3-state			
5074	Synchronizing dual D-type flip-flop/clock driver			
TRANSCEIVERS				
245	Octal transceiver with direction pin; 3-state			
245B	16-bit transceiver with direction pin; 3-state			
245-1	Octal transceiver with direction pin; 3-state			
245A-1	16-bit transceiver with 30 Ω termination resistors and direction pin; 3-state			
500C	18-bit universal bus tranceiver; 3-state			
501A	18-bit universal bus tranceiver; 3-state			
543	16-bit latched transceiver with dual enable; 3-state			
543A	Octal latched transceiver with dual enable; 3-state			
2543	16-bit latched transceiver with dual enable and 30 Ω termination resistors; 3-state			
544	Octal latched transceiver with dual enable; inverting; 3-state			
620	Octal transceiver with dual enable; inverting; 3-state			
623	Octal transceiver with dual enable; non-inverting; 3-state			
640	Octal transceiver with direction pin; inverting; 3-state			
646A	Octal bus transceiver/register; 3-state			
646	16-bit bus transceiver/register; 3-state			
648	Octal bus transceiver/register; inverting; 3-state			
651	Octal bus transceiver/register; inverting; 3-state			
652A	Octal transceiver/register; non-inverting; 3-state			
652	16-bit transceiver/register; non-inverting; 3-state			
657	Octal transceiver with parity generator/checker; 3-state			
833	Octal transceiver with parity generator/checker; 3-state			
853	8-bit transceiver with 9-bit parity checker/generator and flag latch; 3-state			
861	10-bit bus transceiver; 3-state			
863	9-bit bus transceiver; 3-state			
899	9-bit dual latch transceiver with 8-bit parity generator/checker; 3-state			
899	16-bit dual latch transceiver with 8-bit parity generator/checker; 3-state			
952A	Dual octal registered transceiver			
1543	Dual octal latched transceiver with dual enable and clear; 3-state			
2052	16-bit registered transceiver; 3-state			
2245	Octal transceiver with direction pin; 3-state			
2245	16-bit transceiver with direction pin; 3-state			
2543	16-bit latched transceiver with dual enable; 3-state			
2623	16-bit transceiver with dual enable; non-inverting; 3-state			
2646	16-bit bus transceiver/register; 3-state			
2652	16-bit transceiver/register; non-inverting; 3-state			
2861	Dual 10-bit bus transceiver; 3-state			
2952	Octal registered tranceiver; 3-state			
2953	Octal registered tranceiver; inverting; 3-state			
3205	10-bit BTL transceiver			