SN74ALVC16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS260 - JANUARY 1993 - REVISED MARCH 1994

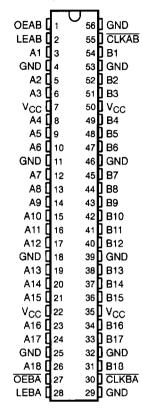
- Member of the Texas Instruments Widebus™ Family
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

DGG OR DL PACKAGE (TOP VIEW)



Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

The SN74ALVC16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16500 is characterized for operation from -40°C to 85°C.

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FUNCTION TABLET

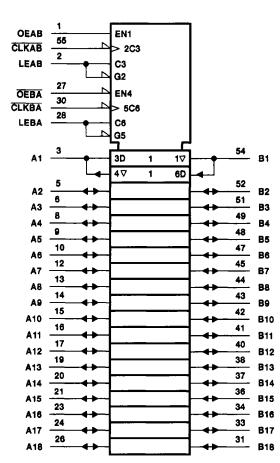
INPUTS			OUTPUT		
OEAB	LEAB	CLKAB	A	В	
L	Х	Х	Χ	Z	
н	Н	Х	L	L	
н	Н	Х	Н	н	
н	L	1	L	L	
н	L	\downarrow	Н	н	
н	L	н	Х	В ₀ ‡	
Н	L	L	X	В ₀ ‡ В ₀ §	

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.



[‡] Output level before the indicated steady-state input conditions were established.

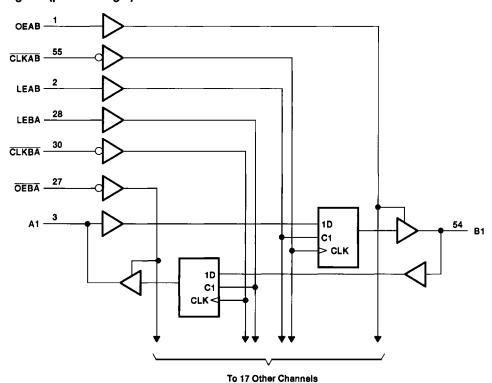
[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3); DGG package	1 W
DL package	
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



PRODUCT PREVIEW

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recommended operating conditions

			MIN	MAX	UNIT	
VCC	Supply voltage		2.7	3.6	٧	
V_{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V	
٧ _I	Input voltage	_	0	Vcc	V	
٧o	Output voltage	 	0	Vcc	V	
ЮН	High level or three courses	V _{CC} = 2.7 V		-12	2	
	High-level output current	V _{CC} = 3 V		-24	mA	
lOL	Law lavel autorit aumant	V _{CC} = 2.7 V	V _{CC} = 2.7 V			
	Low-level output current	V _{CC} = 3 V		24	mA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} t	MIN	MAX	UNIT
Vou		IOH = -100 μA	MIN to MAX	V _{CC} -0.2		
		10.00	2.7 V	2.2		v
VOH	IOH = -12 mA	3 V	2.4		V	
		I _{OH} = -24 mA	3 V	2		
VOL		l _{OL} = 100 μA	MIN to MAX		0.2	
		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V	0.55		
l _l		VI = VCC or GND	3.6 V		±5	μА
	Data I/Os	V _i = 0.8 V	3 V	75		μА
I (hold)		V _I = 2 V		75		
loz‡	_	VO = VCC or GND	3.6 V		±10	μA
lcc_		VI = VCC or GND, IO = 0	3.6 V		40	μA
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND			750	μΑ
Ci	Control inputs	VI = VCC or GND	3.3 V			рF
Cio	A or B ports	VO = VCC or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



For I/O ports, the parameter IOZ includes the input leakage current.