Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS NON-INVERTING BUFFER TRANSCEIVER

ADVANCE INFORMATION
IDT54/74FBT245
IDT54/74FBT245A
IDT54/74FBT245C

FEATURES:

- IDT54/74FBT245 equivalent to the 54/74BCT245
- **IDT54/74FBT245A 25% faster than the 245**
- **IDT54/74FBT245C 10% faster than the 245A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

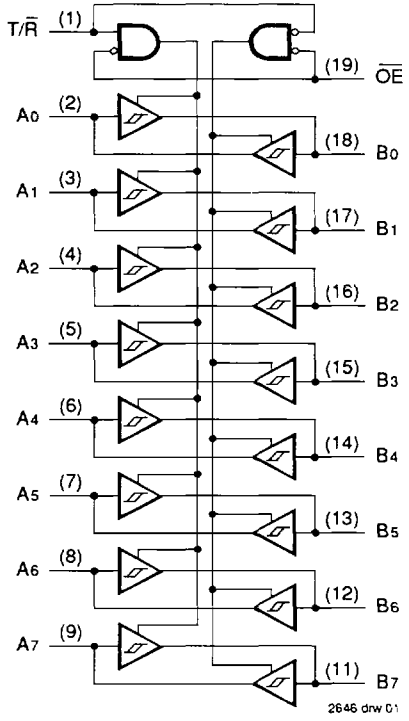
DESCRIPTION:

The FBT series of BiCMOS Buffer Transceivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

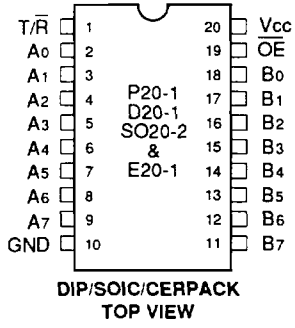
The IDT54/74FBT245 series of 8-bit non-inverting, bidirectional buffers have 3-state outputs and are intended for bus interface applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in the high impedance state.

The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

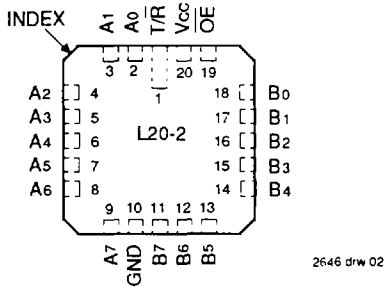
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
$A_0 - A_7$	Side A Inputs or 3-State Outputs
$B_0 - B_7$	Side B Inputs or 3-State Outputs

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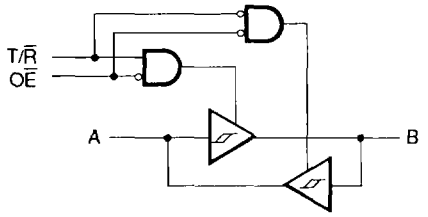
FUNCTION TABLE[1]

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2646 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

LOGIC SYMBOL



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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
2646 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
2646 tbl 04

1. This parameter is measured at characterization but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	—	—	10	µA
		V_I = 2.7V	I/O Pins	—	—	60	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	—	—	-10	µA
		V_I = 0.5V	I/O Pins	—	—	-60	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -12mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15mA COM'L.				
			I_{OH} = -18mA MIL.	2.0	3.0	—	V
			I_{OH} = -24mA COM'L.				
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL.	—	0.3	0.55	V
			I_{OL} = 64mA COM'L.				
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

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NOTES:
1. For conditions shown as Max or Min., use appropriate value specified under Electrical Characteristics for the applicable device type
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND, T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES: 2646 tbl 06

1. For conditions shown as Max or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

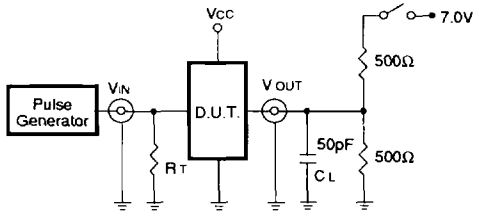
			IDT54/74FBT245				IDT54/74FBT245A				IDT54/74FBT245C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	—	—	1.5	4.9	—	—	1.5	4.1	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	10.9	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	9.1	—	—	1.5	5.0	—	—	1.5	4.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B		1.5	10.9	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B		1.5	9.1	—	—	1.5	5.0	—	—	1.5	4.8	—	—	ns

NOTES: 2646 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

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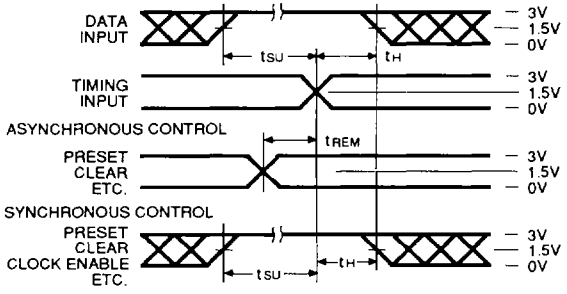
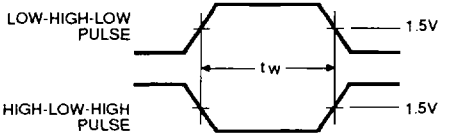
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

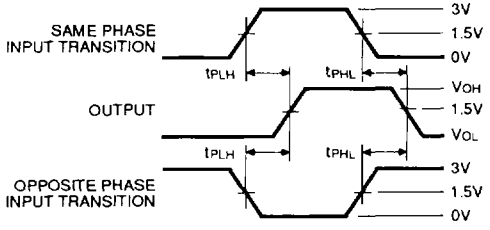
SET-UP, HOLD AND RELEASE TIMES



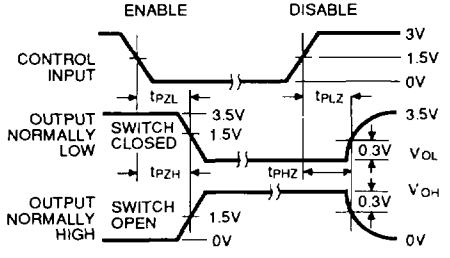
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



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NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns

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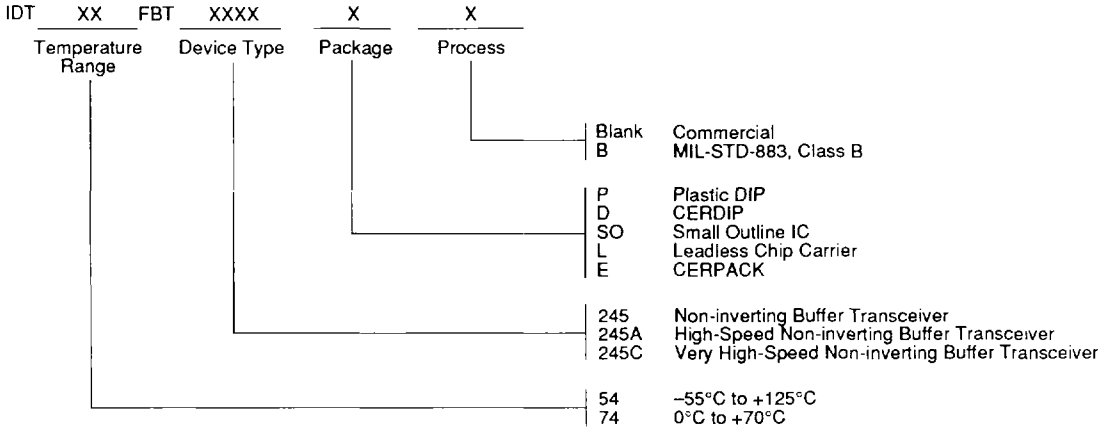
ORDERING INFORMATION



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