

# SN54ACT563, SN74ACT563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS550A – NOVEMBER 1995 – REVISED 1996

- Inputs Are TTL-Voltage Compatible
- 3-State Inverted Outputs Drive Bus Lines Directly
- Flow-Through Architecture to Optimize PCB Layout
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

## description

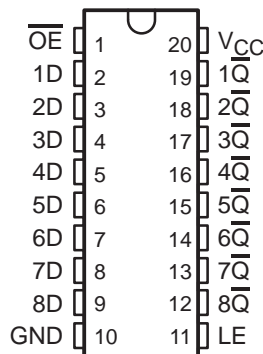
The 'ACT563 are octal D-type transparent latches with 3-state outputs. When the latch-enable (LE) input is high, the  $\bar{Q}$  outputs are set to the complements of the data (D) inputs. When LE is taken low, the  $\bar{Q}$  outputs are latched at the inverse logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

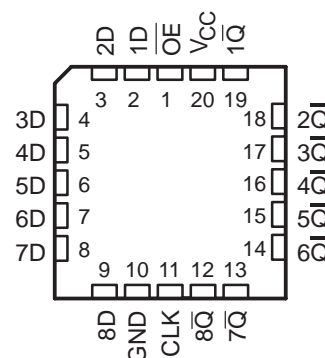
$\overline{OE}$  does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ACT563 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ACT563 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54ACT563 . . . J OR W PACKAGE  
SN74ACT563 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ACT563 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z



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 **TEXAS  
INSTRUMENTS**

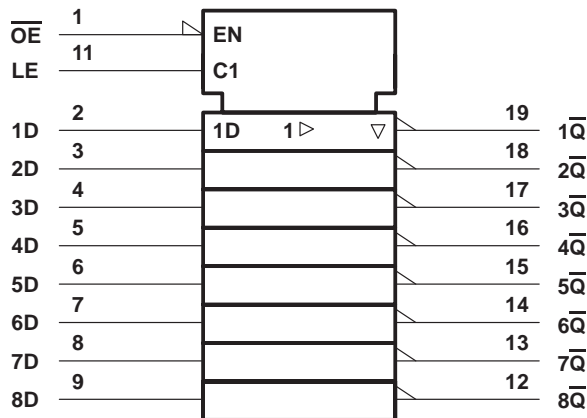
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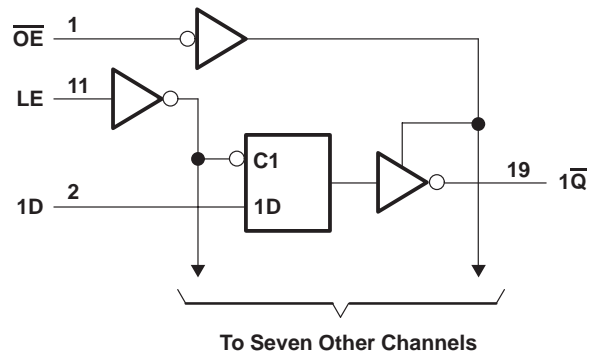
# SN54ACT563, SN74ACT563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package .....	0.6 W
DW package .....	1.6 W
N package .....	1.3 W
PW package .....	0.7 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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## recommended operating conditions (see Note 3)

		SN54ACT563		SN74ACT563		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-24	mA
$I_{OL}$	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54ACT563		SN74ACT563		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.49		4.4		4.4	V	
		5.5 V	5.4	5.49		5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V				3.85				
$I_{OH} = -75 \text{ mA}^\dagger$	5.5 V						3.85			
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V		0.001	0.1		0.1	0.1	V	
		5.5 V		0.001	0.1		0.1	0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V					1.65			
$I_{OL} = 75 \text{ mA}^\dagger$	5.5 V						1.65			
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 5$	$\pm 2.5$	$\mu\text{A}$	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80	40	$\mu\text{A}$	
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V		0.6			1.6	1.5	mA	
$C_i$	$V_I = V_{CC}$ or GND	5 V		4.5					pF	

$^\dagger$  Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

$^\ddagger$  This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

## timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54ACT563		SN74ACT563		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	3		5		3		ns
$t_{su}$	Setup time, data before LE $\downarrow$	4		4.5		4.5		ns
$t_h$	Hold time, data after LE $\downarrow$	0		1.5		0		ns

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**SN54ACT563, SN74ACT563**  
**OCTAL D-TYPE TRANSPARENT LATCHES**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54ACT563		SN74ACT563		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	$\bar{Q}$	3	7	11.5	1	14.5	2.5	12.5	ns
$t_{PHL}$			3	6	10	1	12	2.5	11	
$t_{PLH}$	LE	$\bar{Q}$	3	6.5	10.5	1	12.5	2.5	11.5	ns
$t_{PHL}$			2.5	5.5	9.5	1	11.5	2	10.5	
$t_{PZH}$	$\overline{OE}$	$\bar{Q}$	2.5	5.5	9	1	11.5	2	10	ns
$t_{PZL}$			2	5.5	8.5	1	11	2	9.5	
$t_{PHZ}$	$\overline{OE}$	$\bar{Q}$	3.5	6.5	10.5	1	12	2.5	11.5	ns
$t_{PLZ}$			2	4.5	8	1	9.5	1	8.5	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

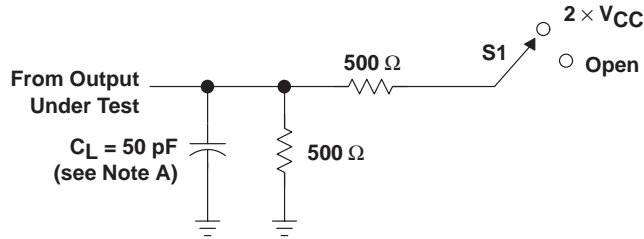
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	50	pF

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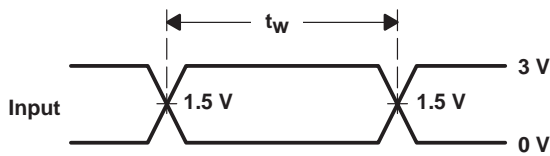
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PARAMETER MEASUREMENT INFORMATION

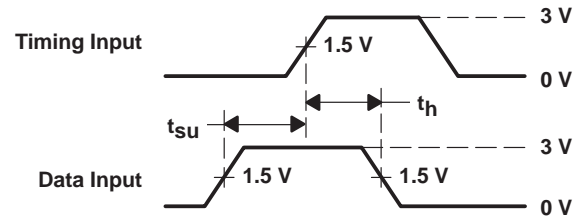


LOAD CIRCUIT

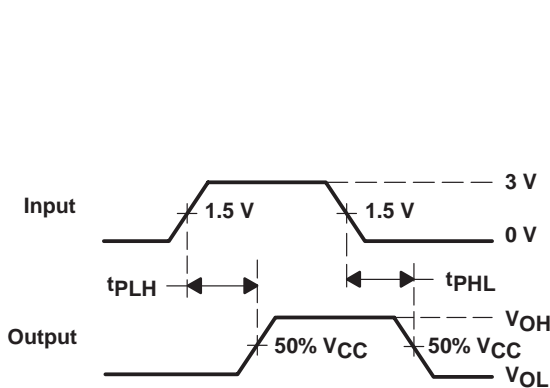
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



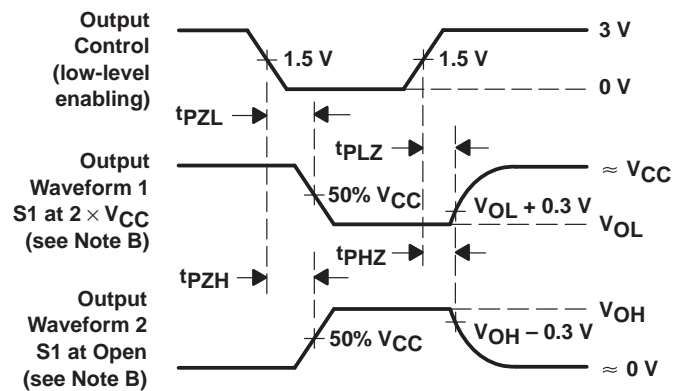
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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## SN74ACT563, Octal D-Type Transparent Latches With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74ACT563
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	CMOS
Output Drive (mA)	-24/24
No. of Outputs	8
Static Current	0.04
th (ns)	0
tpd max (ns)	12.5
tsu (ns)	4.5
Logic	Inv

### FEATURES

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- Inputs Are TTL-Voltage Compatible
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- Flow-Through Architecture to Optimize PCB Layout
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- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

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### DESCRIPTION

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A buffered output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

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**TECHNICAL DOCUMENTS**[▲Back to Top](#)To view the following documents, [Acrobat Reader 4.0](#) is required.

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**DATASHEET**[▲Back to Top](#)Full datasheet in Acrobat PDF: [sn74act563.pdf](#) (109 KB,Rev.A) (Updated: 05/01/1996)**APPLICATION NOTES**[▲Back to Top](#)View Application Notes for [Digital Logic](#)

- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits \(SZZA026\)](#) - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

**RELATED DOCUMENTS**[▲Back to Top](#)View Related Documentation for [Digital Logic](#)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

**SAMPLES**[▲Back to Top](#)

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ACT563DBR	<a href="#">SSOP (DB)</a>	20	-40 TO 85	ACTIVE	<a href="#">View Product Content</a>	<a href="#">Request Samples</a>
SN74ACT563DW	<a href="#">SOP (DW)</a>	20	-40 TO 85	ACTIVE	<a href="#">View Product Content</a>	<a href="#">Request Samples</a>

**PRICING/AVAILABILITY/PKG**[▲Back to Top](#)

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY   \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74ACT563DBLE	OBSOLETE	<a href="#">SSOP (DB)</a>   20	-40 TO 85	<a href="#">View Contents</a>	1KU		<a href="#">N/A*</a>		Not Available			
SN74ACT563DBR	ACTIVE	<a href="#">SSOP (DB)</a>   20	-40 TO 85	<a href="#">View Contents</a>	1KU   0.49	2000	<a href="#">N/A*</a>	> 10k   07 Oct	8 WKS			
								> 10k   14 Oct				
SN74ACT563DW	ACTIVE	<a href="#">SOP (DW)</a>   20	-40 TO 85	<a href="#">View Contents</a>	1KU   0.49	25	<a href="#">N/A*</a>	> 10k   07 Oct	8 WKS			
								> 10k   14 Oct				



SN74ACT563DWR	ACTIVE	<a href="#">SOP (DW)</a>   20	-40 TO 85	<a href="#">View Contents</a>	1KU   0.49	2000	<a href="#">N/A*</a>	1538   03 Oct	8 WKS			
								>10k   04 Oct				
								>10k   11 Oct				
SN74ACT563N	ACTIVE	<a href="#">PDIP (N)</a>   20	-40 TO 85	<a href="#">View Contents</a>	1KU   0.49	20	<a href="#">N/A*</a>	90   19 Sep	8 WKS			
								13   25 Sep				
								>10k   07 Oct				
								>10k   14 Oct				
								>10k   21 Oct				
SN74ACT563NSR	ACTIVE	<a href="#">SOP (NS)</a>   20		<a href="#">View Contents</a>	1KU   0.49	2000	<a href="#">N/A*</a>	>10k   07 Oct	8 WKS			
								>10k   14 Oct				
SN74ACT563PWLE	OBSOLETE	<a href="#">TSSOP (PW)</a>   20	-40 TO 85	<a href="#">View Contents</a>	1KU		<a href="#">N/A*</a>		Not Available			
SN74ACT563PWR	ACTIVE	<a href="#">TSSOP (PW)</a>   20	-40 TO 85	<a href="#">View Contents</a>	1KU   0.49	2000	<a href="#">N/A*</a>	>10k   03 Oct	8 WKS			
								>10k   10 Oct				

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