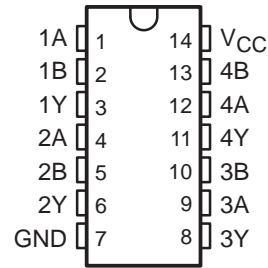


# SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

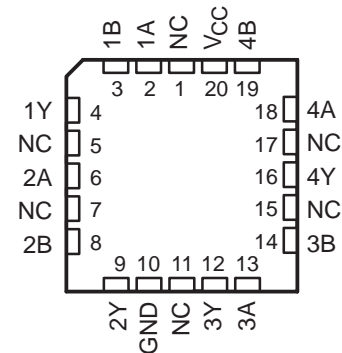
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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V  $V_{CC}$**
- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'AHC00**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54AHC132 . . . J OR W PACKAGE  
SN74AHC132 . . . D, DB, DGV, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHC132 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The 'AHC132 devices are quadruple positive-NAND gates designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices perform the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54AHC132 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC132 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H



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 **TEXAS  
INSTRUMENTS**

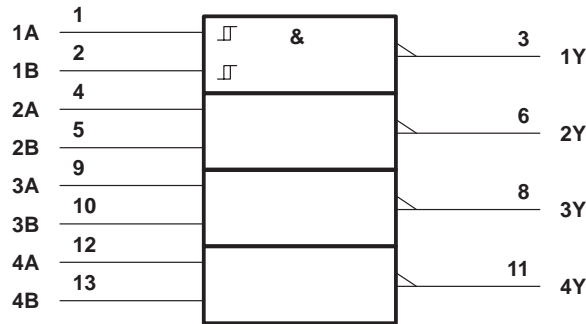
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# SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

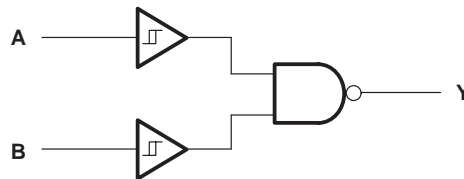
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram, each gate (positive logic)‡



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package .....	86°C/W
DB package .....	96°C/W
DGV package .....	127°C/W
N package .....	80°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

# SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

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## recommended operating conditions (see Note 3)

		SN54AHC132		SN74AHC132		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	-50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-4	-4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		-8	-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4	4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		8	8	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC132		SN74AHC132		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		3 V	1.2		2.2	1.2	2.2	1.2	2.2	V
		4.5 V	1.75		3.15	1.75	3.15	1.75	3.15	
		5.5 V	2.15		3.85	2.15	3.85	2.15	3.85	
V <sub>T-</sub> Negative-going input threshold voltage		3 V	0.9		1.9	0.9	1.9	0.9	1.9	V
		4.5 V	1.35		2.75	1.35	2.75	1.35	2.75	
		5.5 V	1.65		3.35	1.65	3.35	1.65	3.35	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		3 V	0.3		1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20		20	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		1.9	10				10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

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# SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC132		SN74AHC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	5.6*	11.9*	1*	14*	1	14	ns	
$t_{PHL}$				5.6*	11.9*	1*	14*	1	14		
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	7.6	15.4	1	17.5	1	17.5	ns	
$t_{PHL}$				7.6	15.4	1	17.5	1	17.5		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC132		SN74AHC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	3.9*	7.7*	1*	9*	1	9	ns	
$t_{PHL}$				3.9*	7.7*	1*	9*	1	9		
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	5.3	9.7	1	11	1	11	ns	
$t_{PHL}$				5.3	9.7	1	11	1	11		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		SN74AHC132			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.45	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.35	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage		3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

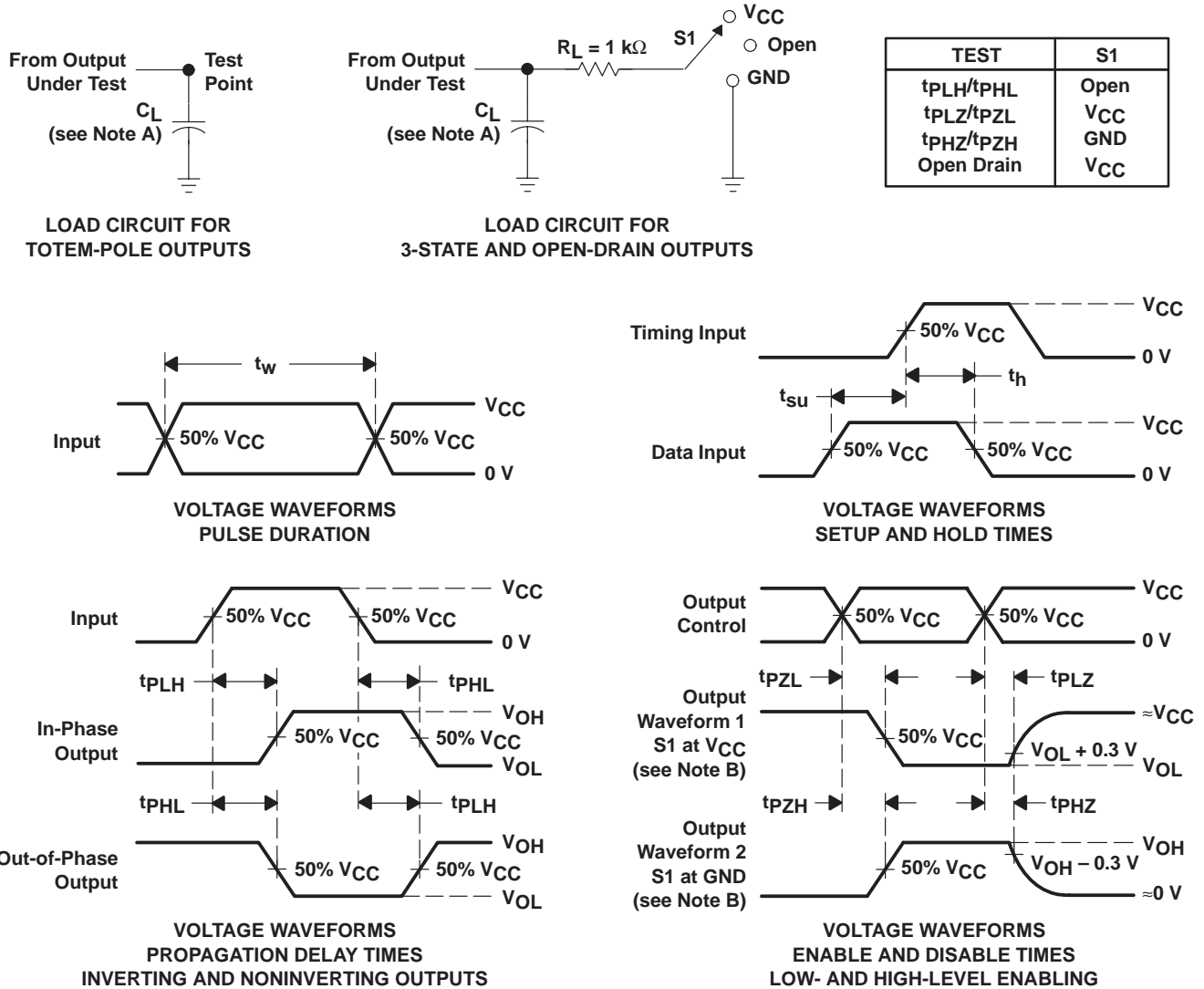
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	11	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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