Octal D-type registered transceiver (3-State) 74LVC543A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8–1A
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State non-inverting outputs for bus oriented applications
- High impedance when V_{CC} = 0V

DESCRIPTION

The 74LVC543A is a high–performance, low–power, low–voltage, Si–gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC543A is an octal registered transceiver containing two sets of D–type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC543A contains eight D–type latches, with separate inputs and controls for each set. For data flow from A to B, for example, the A–to–B enable ($\overline{E}_{AB}$) input must be LOW in order to enter data from A_0–A_7 or take data from B_0–B_7, as indicated in the function table. With $\overline{E}_{AB}$ LOW, a LOW signal on the A–to–B latch enable ($\overline{LE}_{AB}$) input makes the A–to–B latches transparent; a subsequent LOW–to HIGH transition of the $\overline{LE}_{AB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both low, the 3–state B output buffers are active and display the data present at the outputs of the A latches

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $T_r = T_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n	C_L = 50 pF V_{CC} = 3.3V	3.3	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10.0	pF
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3V	27	pF

NOTES:

2. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
3. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG DWG. #
24-Pin Plastic Small Outline (SO)	–40°C to +85°C	74LVC543A D	74LVC543A D	SOT137-1
24-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC543A DB	74LVC543A DB	SOT340-1
24-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC543A PW	7LVC543APW DH	SOT355-1

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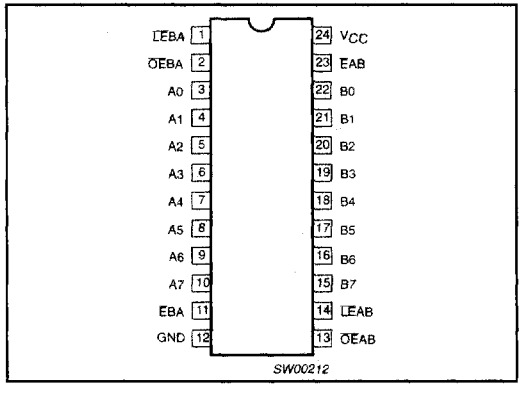
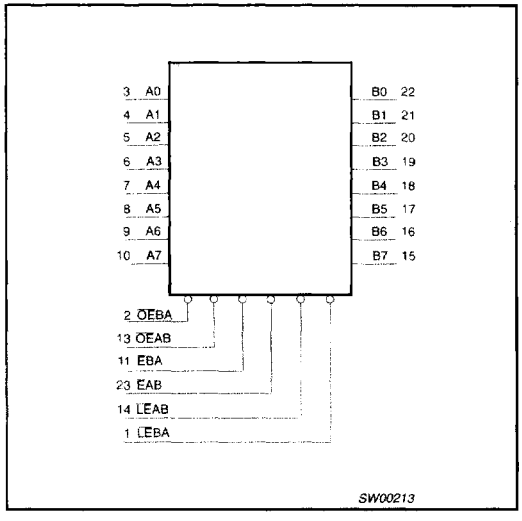
PIN CONFIGURATION



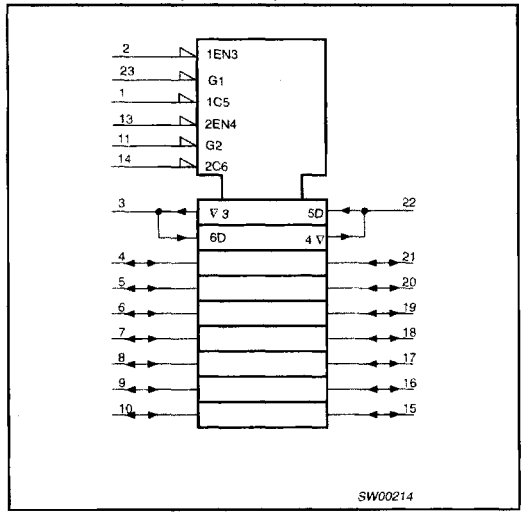
LOGIC SYMBOL



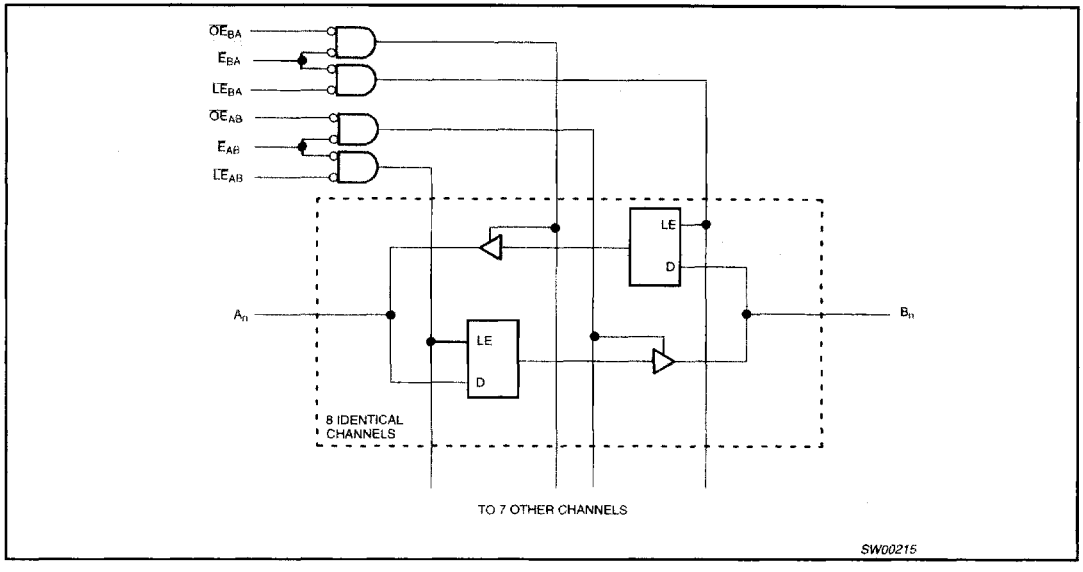
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{LE}_{BA}$	'B' to 'A' latch enable input (active LOW)
2	$\overline{OE}_{BA}$	'B' to 'A' output enable input (active LOW)
3,4,5,6, 7, 8, 9 10	A_0 to A_7	'A' data inputs/outputs
11	$\overline{E}_{BA}$	'B' to 'A' enable input (active LOW)
12	GND	ground (0V)
22, 21, 20, 19, 18, 17, 16, 15	B_0 to B_7	'B' data inputs/outputs
13	$\overline{OE}_{AB}$	'A' to 'B' output enable input (active LOW)
14	$\overline{LE}_{AB}$	'A' to 'B' latch enable input (active LOW)
23	$\overline{E}_{AB}$	'A' to 'B' enable input (active LOW)
24	V_{CC}	positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{OE}_{XX}$	E_{XX}	$\overline{LE}_{XX}$	DATA	
Disabled	H	X	X	X	Z
Disabled	X	H	X	X	Z
Disabled + Latch	L L	↑ ↑	L L	h l	Z Z
Latch + Display	L L	L L	↑ ↑	h l	H L
Transparent	L L	L L	L L	H L	H L
Hold (do nothing)	L	L	H	X	NC

NOTES:

XX = AB for A-to-B direction, BA for B-to-A direction
H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
X = Don't care
↑ = Low-to-High level transition
NC = No change
Z = High impedance OFF state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC Output voltage range: output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	–0.5 to 6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V		V_{CC}			V
		V_{CC} = 2.7 to 3.6V		2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V				GND	V
		V_{CC} = 2.7 to 3.6V				0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA		V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA		V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA		V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA		V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA				0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND	Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = 5.5V or GND			±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND			0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V			0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0			5	500	µA

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ =2.5ns; C_L = 50pF

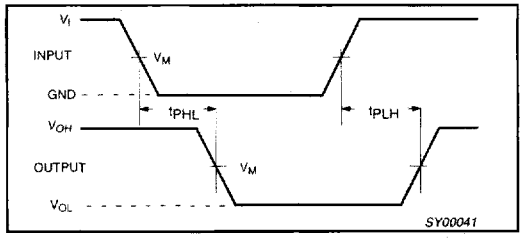
SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay A_n to B_n, B_n to A_n	1, 5	1.5	3.3	7	1.5	8	13.0	ns
t_{PHL} t_{PLH}	Propagation delay $\overline{LE}_{BA}$ to A_n, $\overline{LE}_{AB}$ to B_n,	2, 5	1.5	4.1	8.5	1.5	9.5	16.0	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n,	3, 5	1.5	4.2	7.7	1.5	9.2	15.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n,	3, 5	1.5	3.4	7.0	1.5	7.5	8.0	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{E}_{BA}$ to A_n, $\overline{E}_{AB}$ to B_n,	3, 5	1.5	4.4	8.0	1.5	9.3	15.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{E}_{BA}$ to A_n, $\overline{E}_{AB}$ to B_n,	3, 5	1.5	3.6	7.0	1.5	7.5	8.0	ns
t_W	$\overline{LE}_{XX}$ pulse width LOW	2	3.0	0.9	–	3.0	–	4.0	ns
t_{su}	Set-up time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	4	1.5	–0.5	–	1.5	–	–1.5	ns
t_h	Hold time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	4	1.5	0.6	–	1.5	–	2.0	ns

NOTE:

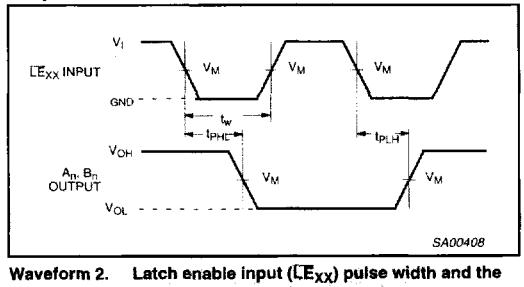
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

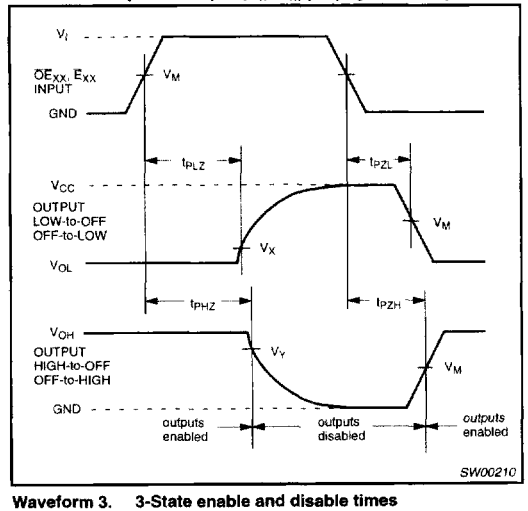
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V



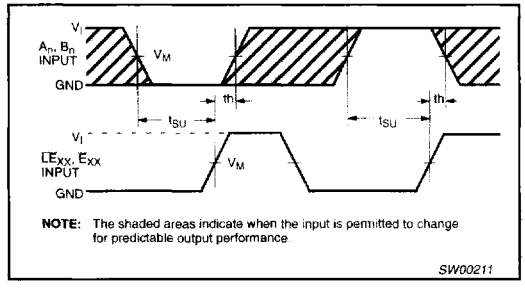
Waveform 1. Input (A_n, B_n) to output (B_n, A_n) propagation delays.



Waveform 2. Latch enable input ($\overline{LE}_{XX}$) pulse width and the latch enable input to output (A_n, B_n) propagation delays.

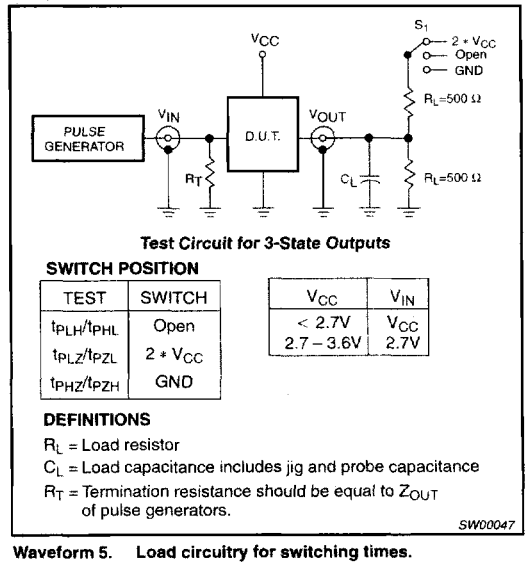


Waveform 3. 3-State enable and disable times



Waveform 4. Data setup and hold times for the (A_n, B_n) input to the $\overline{LE}_{XX}$ and $\overline{E}_{XX}$ inputs.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times.