

# SN54HC390, SN54HC393, SN74HC390, SN74HC393 DUAL 4-BIT DECADE AND BINARY COUNTERS

D2684, DECEMBER 1982—REVISED JUNE 1989

- 'HC390...Individual Clock for A and B Flip-Flops Provide Dual + 2 and + 5 Counters
- 'HC393...Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

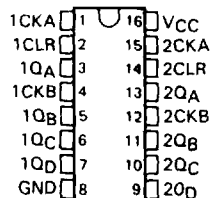
## description

Each of these monolithic circuits contains eight flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'HC390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'HC393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The 'HC390 and 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

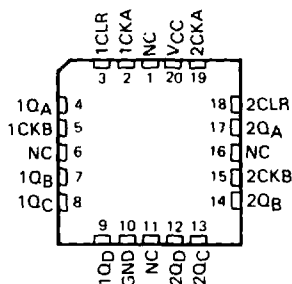
The SN54HC390 and SN54HC393 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC390 and SN74HC393 are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

†Contact the factory for D availability.

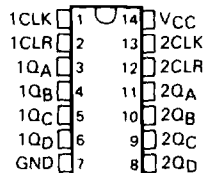
SN54HC390 ... J PACKAGE  
SN74HC390 ... D† OR N PACKAGE  
(TOP VIEW)



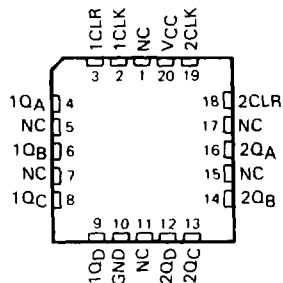
SN54HC390 ... FK PACKAGE  
(TOP VIEW)



SN54HC393 ... J PACKAGE  
SN74HC393 ... N PACKAGE  
(TOP VIEW)



SN54HC393 ... FK PACKAGE  
(TOP VIEW)



NC No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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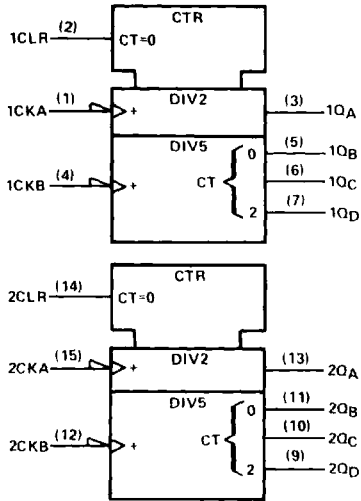
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**SN54HC390, SN74HC390**  
**DUAL 4-BIT DECADE COUNTERS**

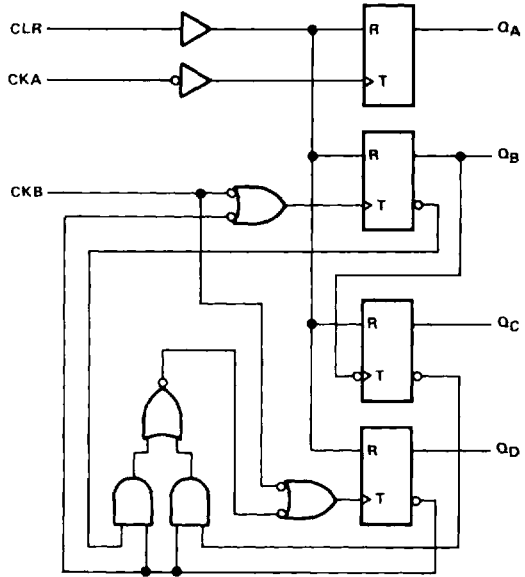
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

logic diagram, each counter (positive logic)



**FUNCTION TABLES**

**BCD COUNT SEQUENCE**  
**(EACH COUNTER)**  
 (See Note A)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

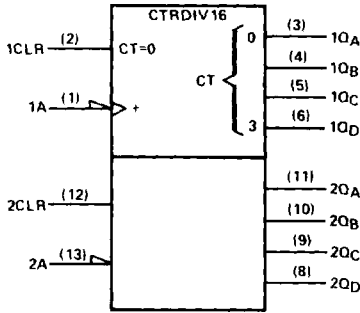
**BIQUINARY (5-2)**  
**(EACH COUNTER)**  
 (See Note B)

COUNT	OUTPUT			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Notes: A. Output Q<sub>A</sub> is connected to input CKB for BCD count.  
 B. Output Q<sub>D</sub> is connected to input CKA for biquinary count.  
 H = high level, L = low level.

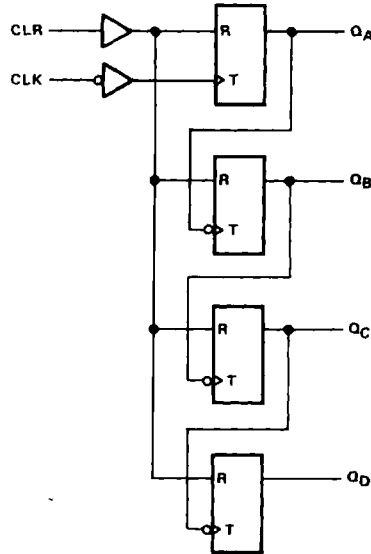
**SN54HC393, SN74HC393**  
**DUAL 4-BIT BINARY COUNTERS**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 817-12. Pin numbers shown are for J and N packages.

logic diagram, each counter (positive logic)



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FUNCTION TABLE  
 COUNT SEQUENCE  
 (EACH COUNTER)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

# SN54HC390, SN54HC393, SN74HC390, SN74HC393 DUAL 4-BIT DECADE AND BINARY COUNTERS

## absolute maximum ratings over operating free-air temperature range†

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND pins .....	$\pm 50$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package .....	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package .....	260°C
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54HC390 SN54HC393			SN74HC390 SN74HC393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5			V
		$V_{CC} = 4.5$ V	3.15		3.15			
		$V_{CC} = 6$ V	4.2		4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0	0.3	0	0.3		V
		$V_{CC} = 4.5$ V	0	0.9	0	0.9		
		$V_{CC} = 6$ V	0	1.2	0	1.2		
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000	0	1000		ns
		$V_{CC} = 4.5$ V	0	500	0	500		
		$V_{CC} = 6$ V	0	400	0	400		
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

**SN54HC390, SN54HC393, SN74HC390, SN74HC393  
DUAL 4-BIT DECADE AND BINARY COUNTERS**

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25 °C			SN54HC390 SN54HC393		SN74HC390 SN74HC393		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> . I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> . I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.80		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> . I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	4.5 V		0.17	0.26		0.4		0.33		
	6 V		0.15	0.26		0.4		0.33		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> . I <sub>OL</sub> = 5.2 mA	6 V								
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8		160		80	μA
C <sub>I</sub>		2 to 6 V		3	10		10		10	pF

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25 °C			SN54HC390		SN74HC390		UNIT
			MIN		MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	CKA	2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	20	0	25	
			6 V	0	36	0	25	0	28	
	CKB	2 V	0	6	0	4.2	0	5		
		4.5 V	0	31	0	20	0	25		
		6 V	0	36	0	25	0	28		
t <sub>w</sub>	Pulse duration	CKA high or low	2 V	80		120		100	ns	
			4.5 V	16		24		20		
			6 V	14		20		18		
		CKB high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		18		
	CLR high	2 V	80		120		100			
		4.5 V	16		24		20			
		6 V	14		20		18			
t <sub>su</sub>	Setup time, CLR inactive	2 V		25		25		25		
		4.5 V		5		5		5		
		6 V		5		5		5		

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**SN54HC390, SN74HC390**  
**DUAL 4-BIT BINARY COUNTERS**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50$  pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC390		SN74HC390		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CKA	Q <sub>A</sub>	2 V	6	10		4.2	5	MHz		
			4.5 V	31	50		20	25			
			6 V	38	60		25	28			
	CKB	Q <sub>B</sub>	2 V	6	10	4.2	5				
			4.5 V	31	50	20	25				
			6 V	38	60	25	28				
t <sub>pd</sub>	CKA	Q <sub>A</sub>	2 V		50	120		180	150	ns	
			4.5 V		16	24		35	35		
			6 V		13	20		31	26		
t <sub>pd</sub>	CKB	Q <sub>B</sub>	2 V		58	130		195	165	ns	
			4.5 V		18	26		39	33		
			6 V		15	22		33	28		
t <sub>pd</sub>	CKB	Q <sub>C</sub>	2 V		83	185		280	230	ns	
			4.5 V		26	37		55	46		
			6 V		21	32		48	40		
t <sub>pd</sub>	CKB	Q <sub>D</sub>	2 V		60	130		195	160	ns	
			4.5 V		18	26		39	33		
			6 V		14	22		33	28		
t <sub>PHL</sub>	CLR	Any	2 V		45	165		250	205	ns	
			4.5 V		17	33		49	41		
			6 V		14	28		42	35		
t <sub>t</sub>		Any	2 V		28	75		110	95	ns	
			4.5 V		8	15		22	19		
			6 V		6	13		19	16		

C <sub>pd</sub>	Power dissipation capacitance per counter	No load, T <sub>A</sub> = 25°C	40 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.

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**SN54HC393, SN74HC393**  
**DUAL 4-BIT BINARY COUNTERS**

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

			V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC393		SN74HC393		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	CLK	2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	28	
t <sub>w</sub>	Pulse duration	CLK high or low	2 V	80		120		100	ns	
			4.5 V	16		24		20		
			6 V	14		20		18		
		CLR high	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		18		
t <sub>su</sub>	Setup time, CLR inactive		2 V	25		25		25	ns	
			4.5 V	5		5		5		
			6 V	5		5		5		

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C<sub>L</sub> = 50 pF (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLK	Q <sub>A</sub>	2 V	6	10		4.2		5	MHz	
			4.5 V	31	50		21		25		
			6 V	36	60		25		28		
t <sub>pd</sub>	CLK	Q <sub>A</sub>	2 V		50	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		13	20		31		26	
t <sub>pd</sub>	CLK	Q <sub>B</sub>	2 V		72	190		285		240	ns
			4.5 V		22	38		57		47	
			6 V		18	32		48		40	
t <sub>pd</sub>	CLK	Q <sub>C</sub>	2 V		91	240		360		300	ns
			4.5 V		28	48		72		60	
			6 V		22	41		61		51	
t <sub>pd</sub>	CLK	Q <sub>D</sub>	2 V		100	290		430		360	ns
			4.5 V		32	58		87		72	
			6 V		24	50		74		62	
t <sub>PHL</sub>	CLR	Any	2 V		45	165		250		205	ns
			4.5 V		17	33		49		41	
			6 V		14	28		42		35	
t <sub>t</sub>		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C <sub>pd</sub>	Power dissipation capacitance per counter	No load, T <sub>A</sub> = 25°C	40 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.

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