ANALOG DEVICES

LC²MOS
High Speed, Quad SPST Switch

ADG201HS

FEATURES

50ns max Switching Time Over Full Temperature Range
Low R_{ON} (30Ω typ)
Single Supply Specifications for +10.8V to +16.5V Operation
Extended Plastic Temperature Range (−40°C to +85°C)
Break-Before-Make Switching
Low Leakage (100pA typ)
44V Supply max Rating
Available in 16-Lead DIP/SOIC and 20-Lead LCCC/PLCC Packages
ADG201HS (K, B, T) Replaces HI-201HS
ADG201HS (J, A, S) Replaces DG271

GENERAL DESCRIPTION

The ADG201HS is a monolithic CMOS device comprising four independently selectable SPST switches. It is designed on an enhanced LC²MOS process which gives very fast switching speeds and low R_{ON}.

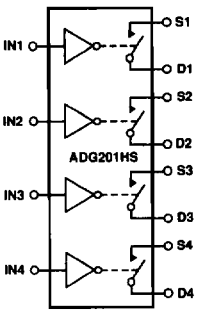
The switches also feature break-before-make switching action for use in multiplexer applications and low charge injection for minimum transients on the output when switching the digital inputs.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG201HSJN	−40°C to +85°C	N-16
ADG201HSKN	−40°C to +85°C	N-16
ADG201HSKR	−40°C to +85°C	R-16
ADG201HSAQ	−40°C to +85°C	Q-16
ADG201HSBQ	−40°C to +85°C	Q-16
ADG201HSJP	−40°C to +85°C	P-20A
ADG201HSKP	−40°C to +85°C	P-20A
ADG201HSSQ	−55°C to +125°C	Q-16
ADG201HSTQ[3]	−55°C to +125°C	Q-16
ADG201HSTE[3]	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See the Analog Devices Military Products Databook (1994) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.
[3]Standard Military Drawing (SMD) approved by DESC. SMD numbers are
5962-86716012X (ADG201HSTE/883B)
5962-8671601EX (ADG201HSTQ/883B)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. 50ns max t_{ON} and t_{OFF}:
The ADG201HS top grades (K, B, T) have guaranteed 50ns max turn-on and turn-off times over the full operating temperature range. The lower grades (J,A,S) have guaranteed 75ns switching times over the full operating temperature range.

2. Single Supply Specifications:
The ADG201HS is fully specified for applications which require a single positive power supply in the +10.8V to +16.5V range.

3. Low Leakage:
Leakage currents in the range of 100pA make these switches suitable for high precision circuits. The added feature of break-before-make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

IN	Switch Condition
0	ON
1	OFF

Truth Table

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

DUAL SUPPLY (V_{DD} = +13.5V to +16.5V, = −13.5V to −16.5V, GND = 0V, V_{IN} 3V [Logic High Level] or 0.8 V [Logic Low Level] unless otherwise noted)

Parameter	Version	+25°C	T_{min}–T_{max}[1]	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	Vmin	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	30	–	Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA; Test Circuit 1
	All	50	75	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	−10V≤V_S≤+10V, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[2]	All	0.1		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[2]	All	0.1		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S,T	1	60	nA max	
I_D (ON), On Channel Leakage[2]	All	0.1		nA typ	V_D = V_S = ±14V; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S,T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF1}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	t_{ON}–t_{OFF1}; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
I_{SS}	All	6	6	mA max	
Power Dissipation	All	240	240	mW max	V_{DD} = +15V, V_{SS} = −15V

NOTES

[1]Temperature ranges are as follows: ADG201HSJ, K; −40°C to +85°C
ADG201HSA, B; −40°C to +85°C
ADG201HSS, T; −55°C to +125°C

[2]Leakage specifications apply with a V_D (V_S) of ±14V or with a V_D (V_S) of 0.5V within the supply voltages (V_{DD}, V_{SS}), whichever is the minimum.

Specifications subject to change without notice.

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SINGLE SUPPLY (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V, V_{IN} = 3V [Logic High Level] or 0.8V [Logic Low Level] unless otherwise noted)

Parameter	Version	+25°C	T_{min}–T_{max}	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	V min	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	65	–	Ω typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	All	90	120	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; V_S = +0.5V/+10V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; V_S = +0.5V/+10V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (ON), On Channel Leakage[1]	All	0.1		nA typ	$V_D = V_S$ = +10V/+0.5V; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF1}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	t_{ON}–t_{OFF1}; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
Power Dissipation	All	150	150	mW max	V_{DD} = +15V

NOTE
[1]The leakage specifications degrade marginally (typically 1nA at 25°C) with V_D (V_S) = V_{SS}.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} 44V
V_{DD} to GND . . . . . −0.3V, 25V
V_{SS} to GND[1] . . . . . +0.3V, −25V
Analog Inputs[2]
Voltage at S, D . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D 20mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[2]
Voltage at IN . . . . . V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First

Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commerical (J, K Version) . . . . . −40°C to +85°C
Industrial (A, B Version) . . . . . −40°C to +85°C
Extended (S, T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

NOTES
[1]If V_{SS} is open circuited with V_{DD} and GND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to GND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.
[2]Overvoltage at IN, S or D, will be clamped by diodes. Current should be limited to the maximum rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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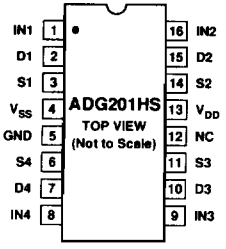
CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

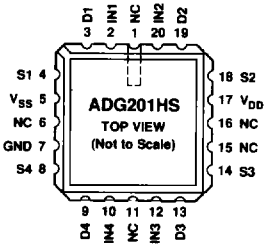
PIN CONFIGURATIONS

DIP, SOIC



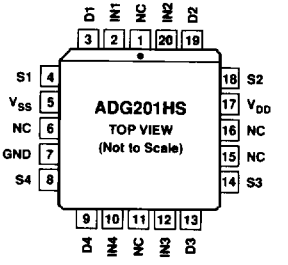
NC = NO CONNECT

LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT