Signetics

FAST 74F827, 74F828
Buffers

FAST Products

74F827 10-Bit Buffer/Line Driver, Non-Inverting (3-State)
74F828 10-Bit Buffer/Line Driver, Inverting (3-State)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **I_{IL} is 20μA vs FAST family spec of 600 A and 1000 A for AMD 29827/29828 series**
- **Ideal where high speed, light bus loading and increased fan-in are required**
- **Controlled rise and fall times to minimize ground bounce**
- **Glitch free power up in 3-state**
- **Flow through pinout architecture for microprocessor oriented applications**
- **Outputs sink 64mA**
- **Slim 300 mil-wide plastic 24-pin package**
- **Pinout and function compatible with AMD 29827/29828 series**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827	6.0ns	60mA
74F828	6.0ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic DIP (300 mil)	N74F827N, N74F828N
24-Pin Plastic SOL	N74F827D, N74F828D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_9	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Q_0- Q_9	Data outputs ('F827)	1200/106.7	24mA/64mA
$\overline{Q}_0$- $\overline{Q}_9$	Data outputs ('F828)	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

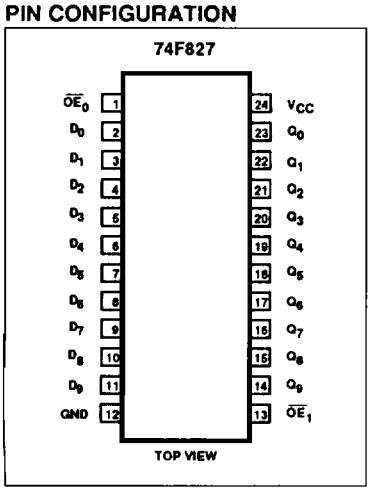
DESCRIPTION

The 74F827 and 74F828 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

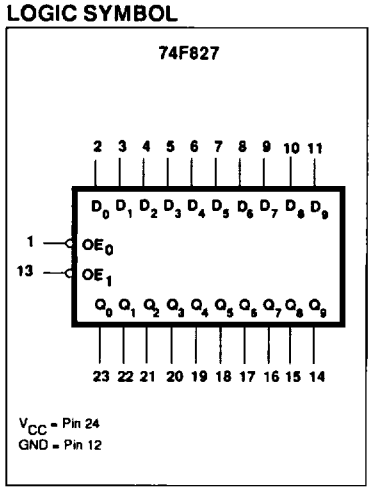
The 'F827 and 'F828 are functionally and pin compatible to AMD AM29827 and AM 29828.

The 'F828 is an inverting version of 'F827.

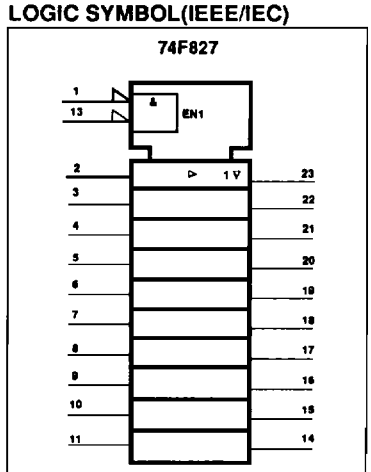
PIN CONFIGURATION



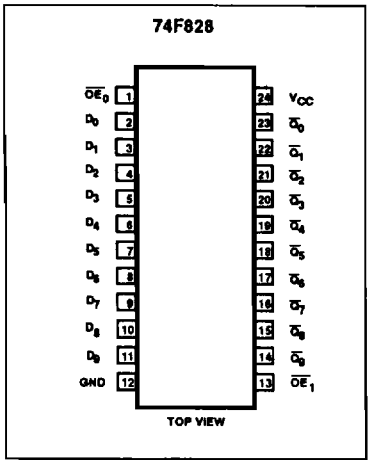
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION



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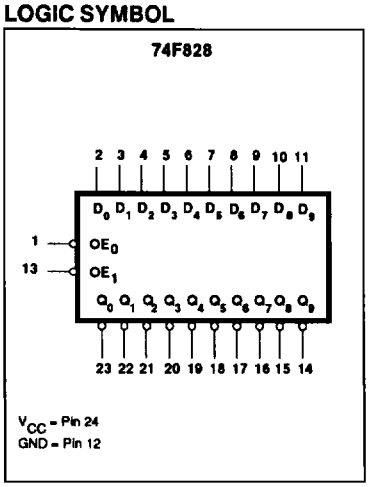

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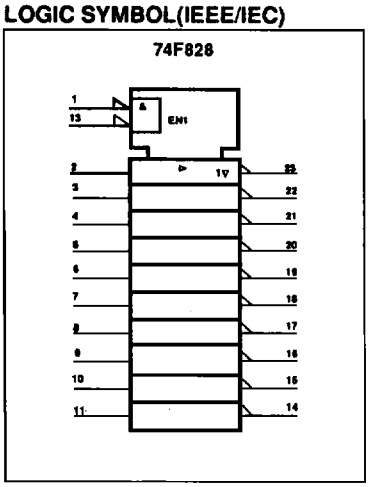
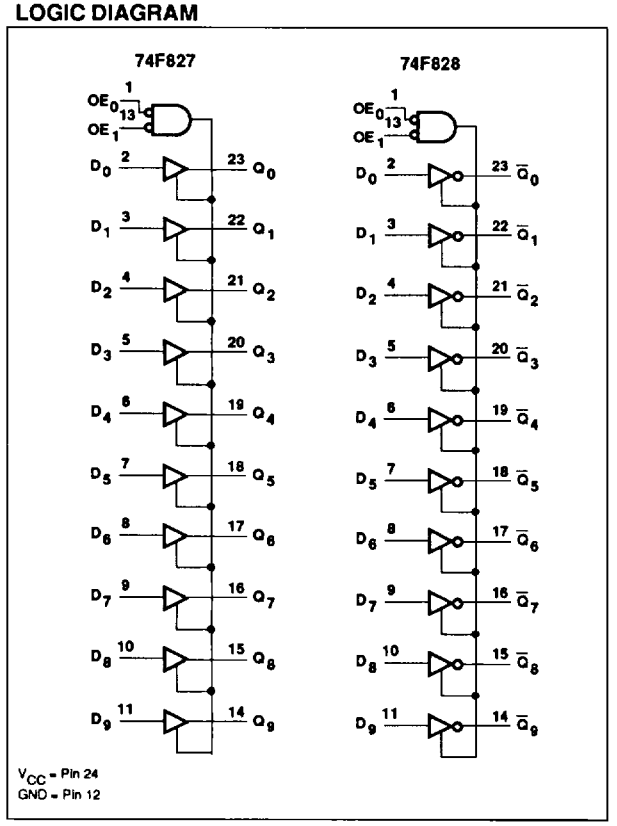


LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
		'827	'828	
$\overline{OE}_n$	D_n	Q_n	$\overline{Q}_n$	
L	L	L	H	Transparent
L	H	H	L	Transparent
H	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.4	3.3		V
		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -24mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F827	I_{CCH}	V_{CC} = MAX		50	70	mA
			I_{CCL}			70	100	mA
			I_{CCZ}			60	90	mA
		'F828	I_{CCH}	V_{CC} = MAX		30	45	mA
			I_{CCL}			65	85	mA
			I_{CCZ}			55	70	mA

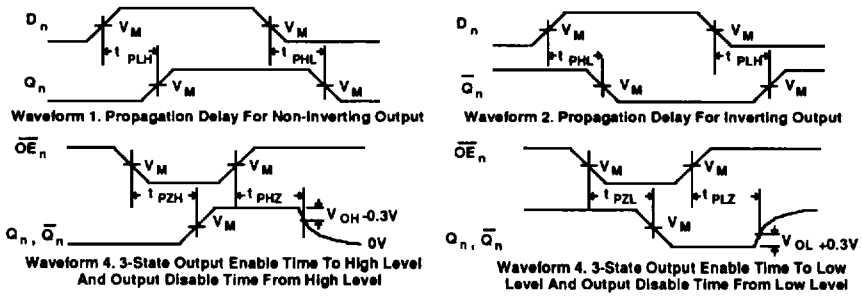
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

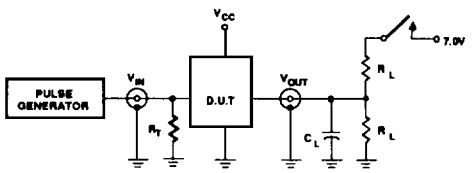
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1	2.0 2.0	5.5 4.5	8.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	5.0 4.0	10.0 7.0	13.5 12.0	4.5 4.0	15.5 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2	2.0 1.0	6.0 3.0	8.5 7.0	2.0 1.0	9.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	7.5 6.5	10.0 8.5	13.0 12.0	7.0 6.0	15.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	2.5 1.5	5.0 4.0	8.5 7.0	2.0 1.5	9.0 8.0	ns

AC WAVEFORMS



NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

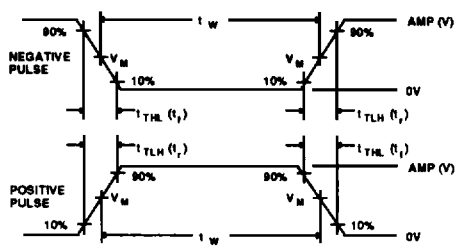
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns