National Semiconductor

DM74ALS125
Quad TRI-STATE® Buffer

General Description

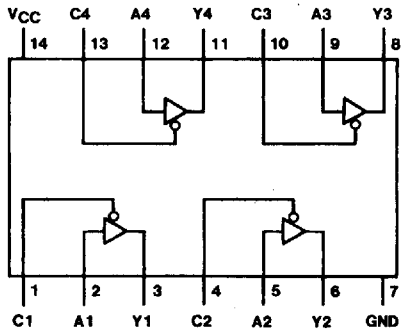
This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the 74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current:
  74ALS = 24 mA

Connection Diagram

Dual-In-Line Package



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Order Number
DM74ALS125N or DM74ALS125M
See NS Package Number M14A or N14A

Functional Table

$Y = A$

Input		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM74ALS	0 to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	78.0°C/W
M Package	111.0°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74ALS125			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Operating Free-Air Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise specified)

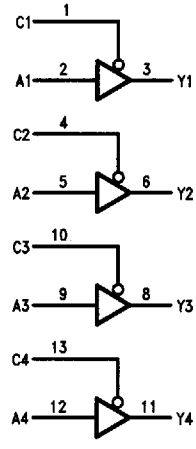
Symbol	Parameter	Conditions		DM74ALS125			Units
				Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			V
			I_{OH} = Max	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		7	10	mA
			Outputs Low		10	14	mA
			TRI-STATE		13.5	18	mA

Switching Characteristics over recommended operating free-air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM74ALS125		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A	Y		2	10	ns
t_{PZH}	Output Enable Time to High Level Output	C	Y		2	13	ns
t_{PZL}	Output Enable Time to Low Level Output	C	Y		2	12	ns
t_{PHZ}	Output Disable Time from High Level Output	C	Y		1	8	ns
t_{PLZ}	Output Disable Time from Low Level Output	C	Y		2	13	ns

Note 1: See Section 5 for test waveforms and output load.

Logic Diagram



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