GD54/74LS112

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

Features

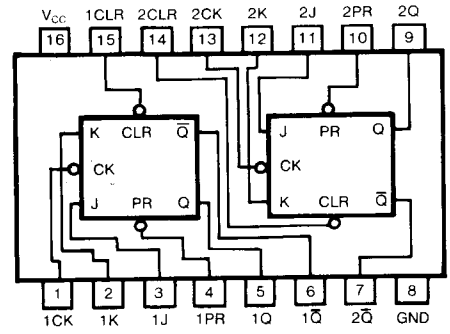
- Negative edge-triggering
- Diode clamped inputs
- Independent input/output terminals for each flip-flop.
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs

Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

↓=Negative Going Edge of Pulse
*=This configuration is nonstable: that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.
Q_O=The output logic level before the indicated input conditions were established.
Toggle=Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Pin Configuration

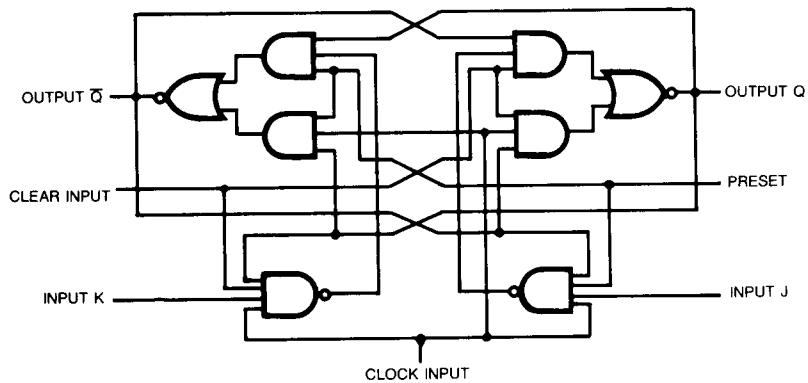


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\overline{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\overline{Q}_O$

Block Diagram (Each Flip Flop)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
t_w	Pulse width	clock high	20		ns
		clock low	25		
		clear or preset low	25		
f_{clock}	Clock frequency		0	30	MHz
t_{su}	Set up time		20↓*		ns
t_h	Input hold time		0↓*		ns
T_A	Operating free-air temperature		0	70	°C

* For falling edge.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	J,K				0.1	mA
			Clear				0.3	
			Preset				0.3	
			Clock				0.4	
I_{IH}	High-level Input current	V_{CC}=Max, V_I=2.7	J,K				20	μA
			Clear				60	
			Preset				60	
			Clock				80	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	J,K				−0.4	mA
			Clear				−0.8	
			Preset				−0.8	
			Clock				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4	6	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from outputs where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O=2.25V and 2.125V for, 54 and 74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, ICC is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			C_L=15 pF, R_L=2KΩ	30	45		MHz
t_{PLH}	Clear, preset Clock	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	

*f_{max}=maximum clock frequency
*t_{PLH}=propagation delay time, low-to-high-level output.
*t_{PHL}=propagation delayt ime, high-to-low-level output.

#For load circuit and voltage waveforms, see page 3-11.