54F/74F113

Dual JK Edge-Triggered Flip-Flop

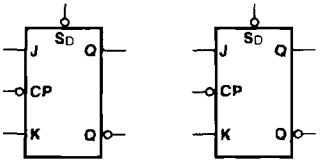
Description

The 'F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

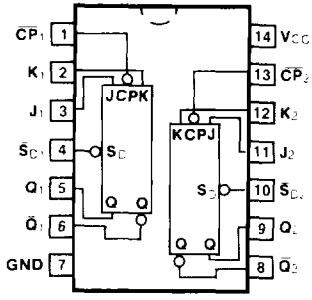
Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

Ordering Code: See Section 5

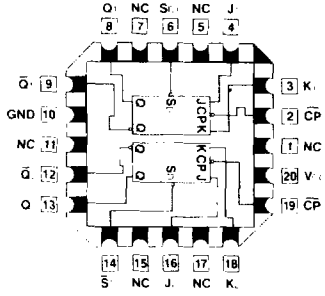
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

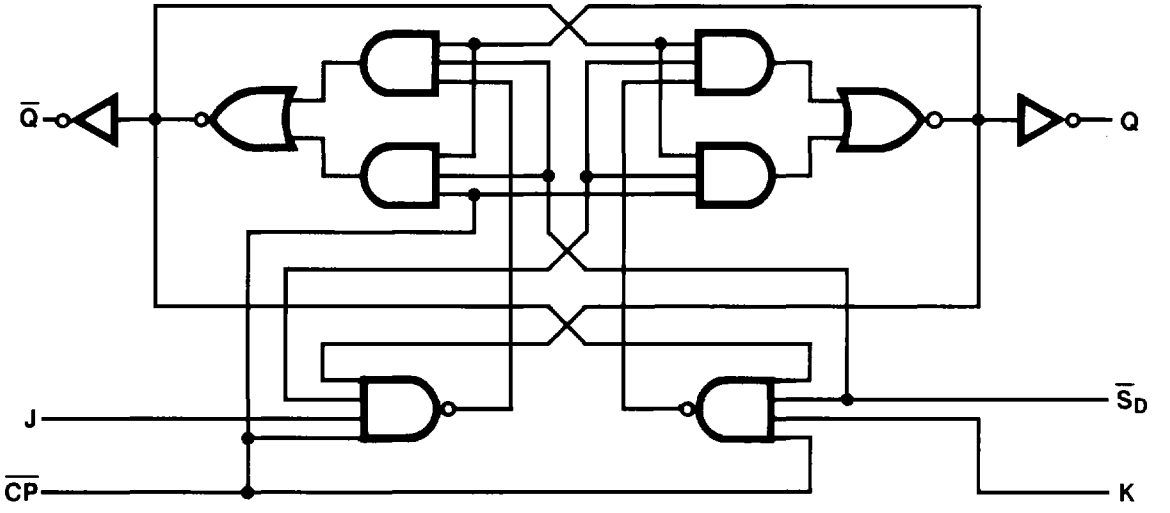
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0.5/1.50
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Truth Table

Inputs		Output
$@t_n$		$@t_{n+1}$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	110	125				100		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0 2.0	4.0 4.0	6.0 6.0			2.0 2.0	7.0 7.0	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0 2.0	4.5 4.5	6.5 6.5			2.0 2.0	7.5 7.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0		5.0 3.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0		0 0		
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse Width HIGH or LOW	4.5 4.5		5.0 5.0	ns	3-8
$t_w(L)$	$\overline{S}_{Dn}$ Pulse Width, LOW	4.5		5.0	ns	3-9
t_{rec}	$\overline{S}_{Dn}$ to $\overline{CP}_n$ Recovery Time	4.0		5.0	ns	3-11

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