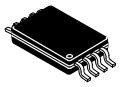
PCS3P624Z05B, PCS3P624Z05C, PCS3P624Z09B, PCS3P624Z09C

Product Preview

High Frequency TIMING SAFE™ Peak EMI Reduction IC

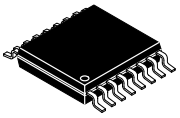
ON Semiconductor®

http://onsemi.com

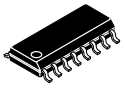


TSSOP−8
T SUFFIX
CASE 948AL

SOIC−8
S SUFFIX
CASE 751BD



TSSOP−16
T SUFFIX
CASE 948AN



SOIC−16
S SUFFIX
CASE 751BG

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

Description

PCS3P624Z05/09 is a versatile, 3.3 V Zero−delay buffer designed to distribute high frequency Timing−Safe clocks with Peak EMI reduction. PCS3P624Z05 is an eight−pin version, accepts one reference input and drives out five low−skew Timing−Safe clocks. PCS3P624Z09 accepts one reference input and drives out nine low−skew Timing−Safe clocks.

PCS3P624Z05/09 has a DLY_CTRL for adjusting the Input−Output clock delay, depending upon the value of capacitor connected at this pin to GND.

PCS3P624Z05/09 operates from a 3.3 V supply and is available in two different packages, as shown in the ordering information table, over commercial and Industrial temperature range.

Application

PCS3P624Z05/09 is targeted for use in Displays and memory interface systems.

Features

- High Frequency Clock Distribution with Timing−Safe Peak EMI Reduction
- Input Frequency Range: 50 MHz − 100 MHz
- Multiple Low Skew Timing−Safe Outputs:
  PCS3P624Z05: 5 Outputs
  PCS3P624Z09: 9 Outputs
- External Input−Output Delay Control Option
- Supply Voltage: 3.3 V ± 0.3 V
- Commercial and Industrial Temperature Range
- Packaging Information:
  ASM3P624Z05: 8 pin SOIC, and TSSOP
  ASM3P624Z09: 16 pin SOIC, and TSSOP
- True Drop−in Solution for Zero Delay Buffer, ASM5P2305A / 09A
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

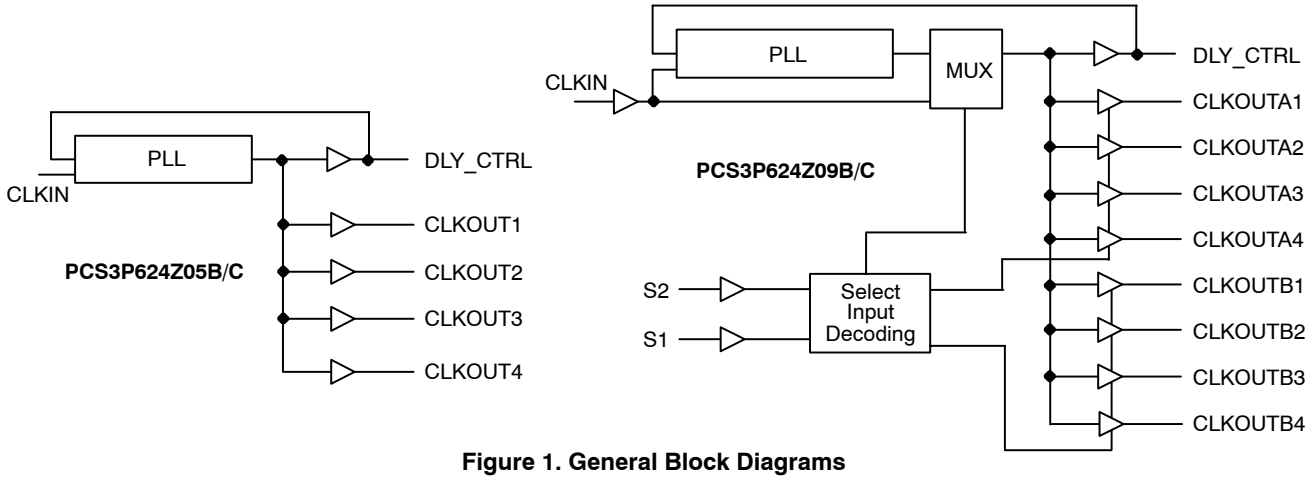


Figure 1. General Block Diagrams

Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi−layer PCBs, etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The PCS3P624Z05/09 uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the DLY_CTRL pin is the internal feedback to the PLL, its relative loading can adjust the input−output delay.

For applications requiring zero input−output delay, all outputs, including DLY_CTRL, must be equally loaded. Even if DLY_CTRL is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero input−output delay.

Timing−Safe Technology

Timing−Safe technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration for PCS3P624Z05B/C

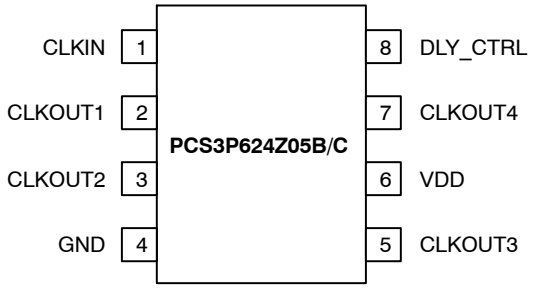


Table 1. PIN DESCRIPTION FOR PCS3P624Z05B/C

Pin #	Pin Name	Type	Description
1	CLKIN (Note 1)	I	External reference Clock input, 5 V tolerant input
2	CLKOUT1 (Note 2)	O	Buffered clock output (Note 4)
3	CLKOUT2 (Note 2)	O	Buffered clock output (Note 4)
4	GND	P	Ground
5	CLKOUT3 (Note 2)	O	Buffered clock output (Note 4)
6	VDD	P	3.3 V supply
7	CLKOUT4 (Note 2)	O	Buffered clock output (Note 4)
8	DLY_CTRL	O	External Input−Output Delay control. This pin can be used as clock output (Note 4)

1. Weak pull down
2. Weak pull−down on all outputs
3. Weak pull−up on these Inputs
4. Buffered clock output is Timing−Safe

Pin Configuration for PCS3P624Z09B/C

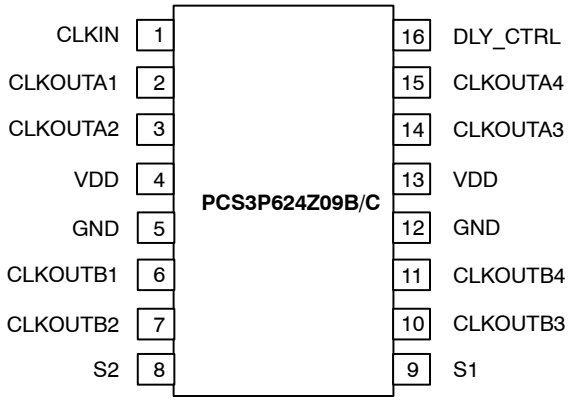


Table 2. PIN DESCRIPTION FOR PCS3P624Z09B/C

Pin #	Pin Name	Pin Type	Description
1	CLKIN (Note 5)	I	External reference Clock input, 5 V tolerant input
2	CLKOUTA1 (Note 6)	O	Buffered clock Bank A output (Note 8)
3	CLKOUTA2 (Note 6)	O	Buffered clock Bank A output (Note 8)
4	VDD	P	3.3 V supply
5	GND	P	Ground
6	CLKOUTB1 (Note 6)	O	Buffered clock Bank B output (Note 8)
7	CLKOUTB2 (Note 6)	O	Buffered clock Bank B output (Note 8)
8	S2 (Note 7)	I	Select input, bit 2. See *Select Input Decoding table for PCS3P624Z09* for more details
9	S1 (Note 7)	I	Select input, bit 1. See *Select Input Decoding table for PCS3P624Z09* for more details
10	CLKOUTB3 (Note 6)	O	Buffered clock Bank B output (Note 8)
11	CLKOUTB4 (Note 6)	O	Buffered clock Bank B output (Note 8)
12	GND	P	Ground
13	VDD	P	3.3 V supply
14	CLKOUTA3 (Note 6)	O	Buffered clock Bank A output (Note 8)
15	CLKOUTA4 (Note 6)	O	Buffered clock Bank A output (Note 8)
16	DLY_CTRL (Note 6)	O	External Input−Output Delay control. This pin can be used as clock output.

5. Weak pull down
6. Weak pull−down on all outputs
7. Weak pull−up on these Inputs
8. Buffered clock output is Timing−Safe

Table 3. SELECT INPUT DECODING TABLE FOR PCS3P624Z09

S2	S1	CLKOUT A1 – A4	CLKOUT B1 – B4	DLY_CTRL (Note 9)	Output Source	PLL Shut–Down
0	0	Three–state	Three–state	Driven	PLL	N
0	1	Driven	Three–state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

9. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the Output.

Table 4. SPREAD SPECTRUM CONTROL AND INPUT–OUTPUT SKEW TABLE

Frequency (MHz)	Device	Deviation (±%)	Input–Output Skew (±T_{SKEW}) (Note 10)
75	PCS3P624Z05B / 09B	0.25	0.0625
	PCS3P624Z05C / 09C	0.5	0.125

10. T_{SKEW} is measured in units of the Clock Period.

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage to Ground Potential	–0.5 to +4.6	V
VIN	DC Input Voltage (CLKIN)	–0.5 to +7	
T_{STG}	Storage temperature	–65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22– A114–B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 6. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	+85	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Table 7. ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage (Note 11)				0.8	V
V_{IH}	Input HIGH Voltage (Note 11)		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0 V			50	μA
I_{IH}	Input HIGH Current	V_{IN} = VDD			100	μA
V_{OL}	Output LOW Voltage (Note 12)	I_{OL} = 8 mA			0.4	V
V_{OH}	Output HIGH Voltage (Note 12)	I_{OH} = −8 mA	2.4			V
I_{DD}	Dynamic Supply Current	Unloaded outputs			40	mA
Z_o	Output Impedance			23		Ω

11. CLKIN input has a threshold voltage of VDD/2
12. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 8. SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Frequency		50		100	MHz
Output Frequency	30 pF load	50		100	MHz
Duty Cycle = (t_2 / t_1) * 100 (Notes 13, 14)	Measured at VDD/2	40	50	60	%
Output Rise Time (Notes 13, 14)	Measured between 0.8 V and 2.0 V			2.5	nS
Output Fall Time (Notes 13, 14)	Measured between 2.0 V and 0.8 V			2.5	nS
Output−to−output skew (Notes 13, 14)	All outputs equally loaded			250	pS
Delay, CLKIN Rising Edge to CLKOUT Rising Edge (Note 14)	Measured at VDD/2			±350	pS
Device−to−Device Skew (Note 14)	Measured at VDD/2 on the CLKOUT pins of the device			700	pS
Cycle−to−Cycle Jitter (Notes 13, 14)	Loaded outputs			±200	pS
PLL Lock Time (Note 14)	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

13. All parameters specified with 30 pF loaded outputs.
14. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

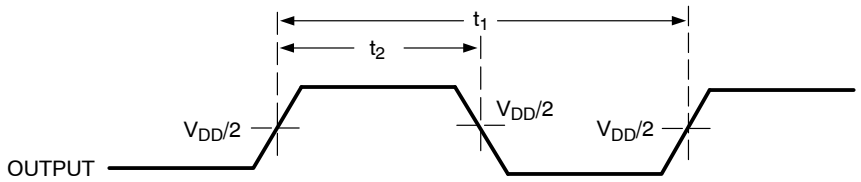


Figure 2. Duty Cycle Timing

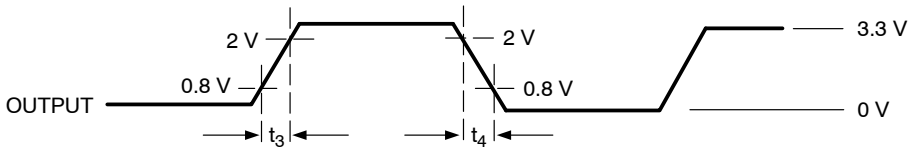


Figure 3. All Outputs Rise/Fall Time

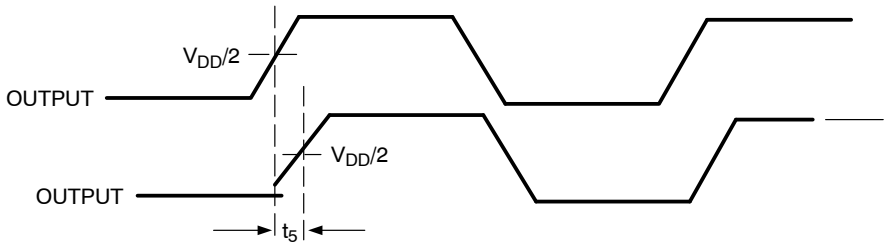


Figure 4. Output − Output Skew

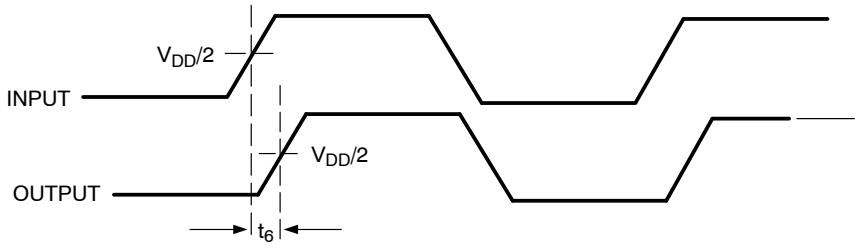


Figure 5. Input − Output Propagation Delay

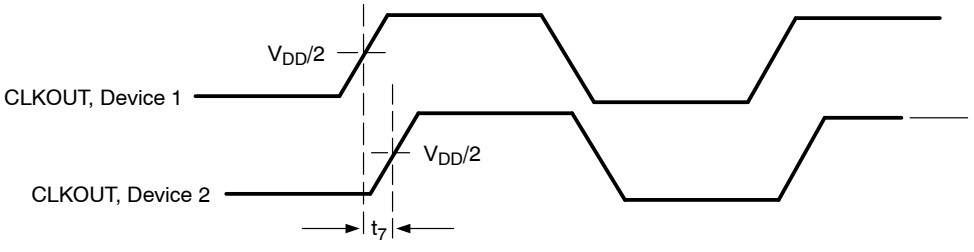


Figure 6. Device − Device Skew

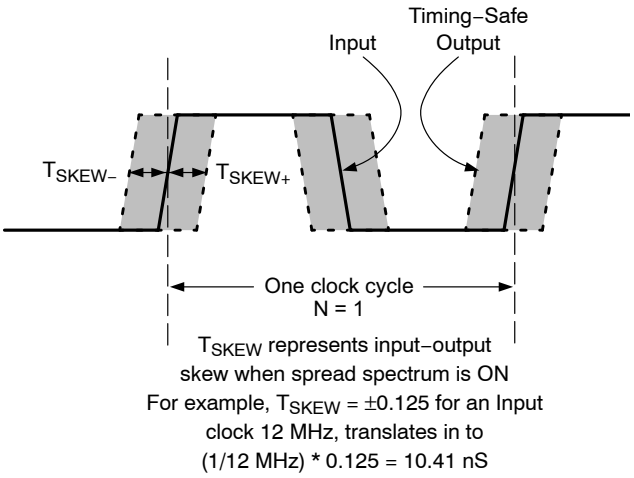


Figure 7. Input − Output Skew

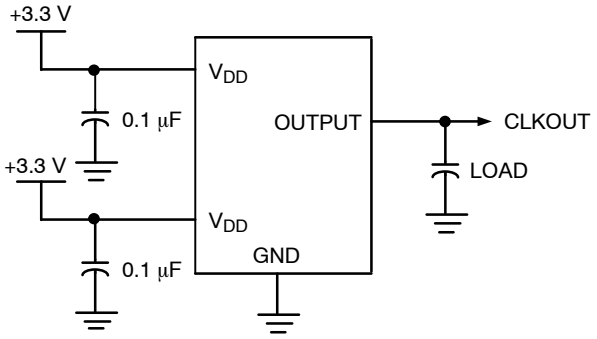
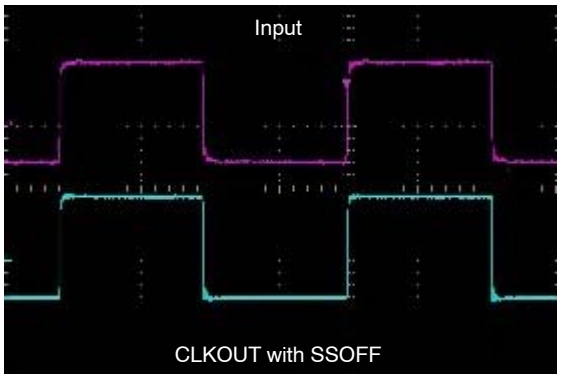


Figure 8. Test Circuit



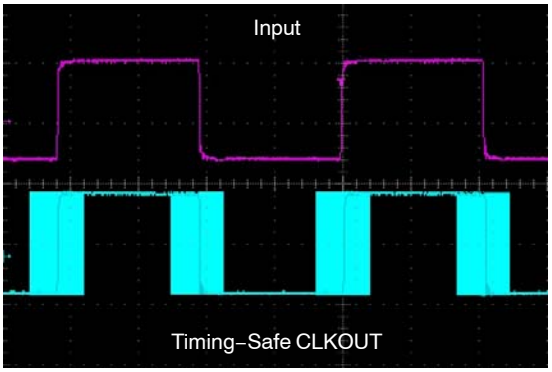
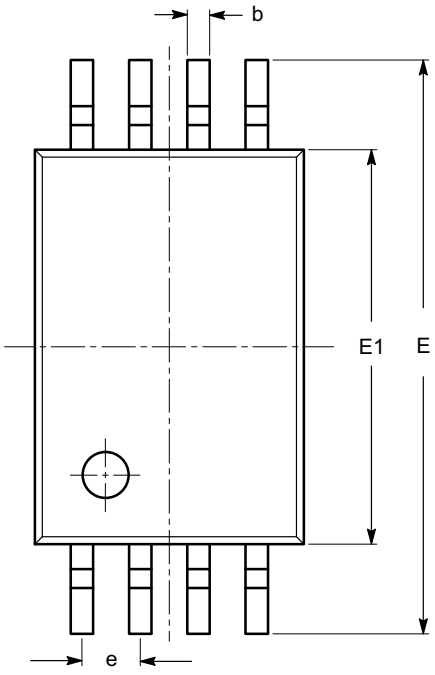


Figure 9. Typical Example of Timing−Safe Waveform

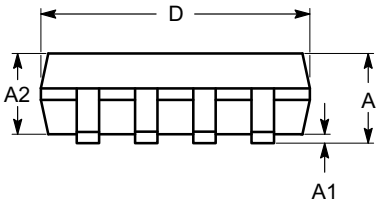
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

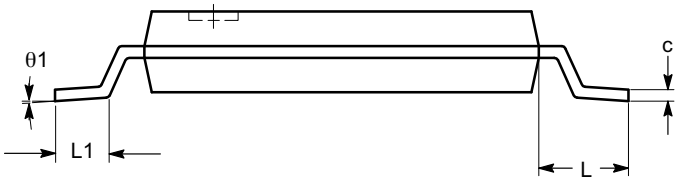


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



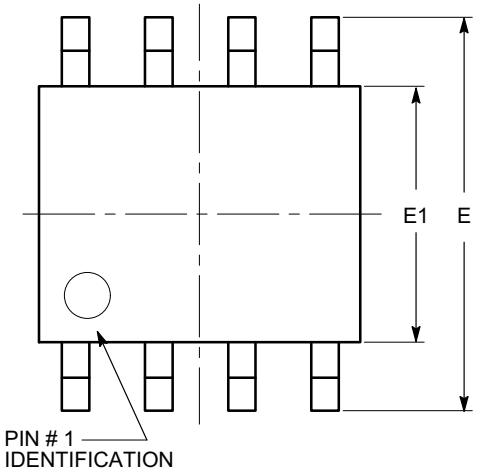
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

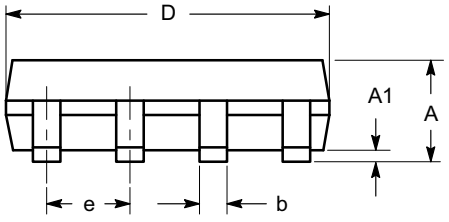
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

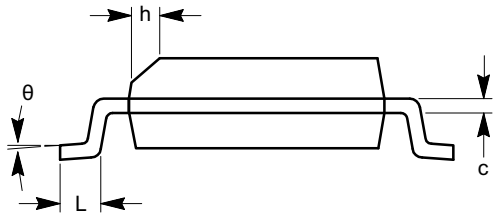


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

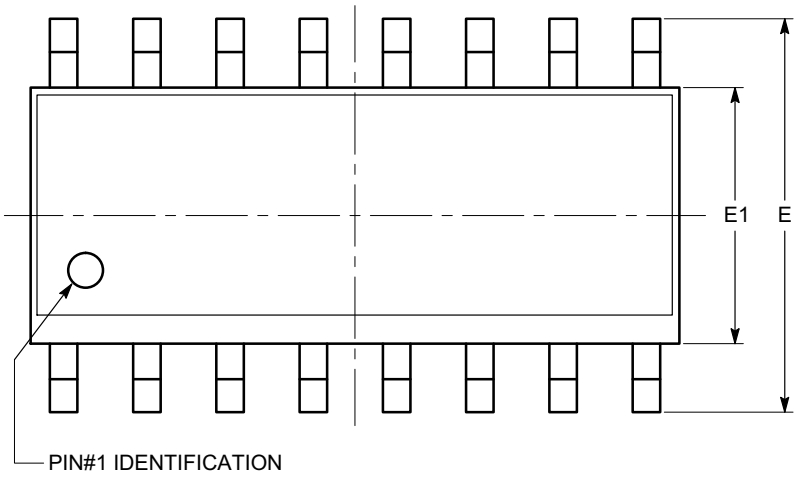


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

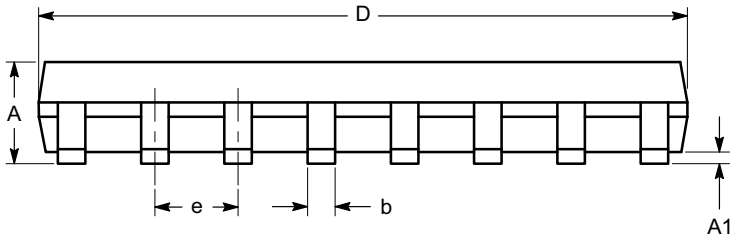
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

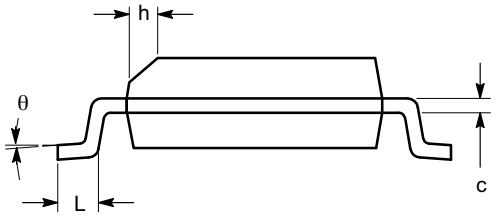


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

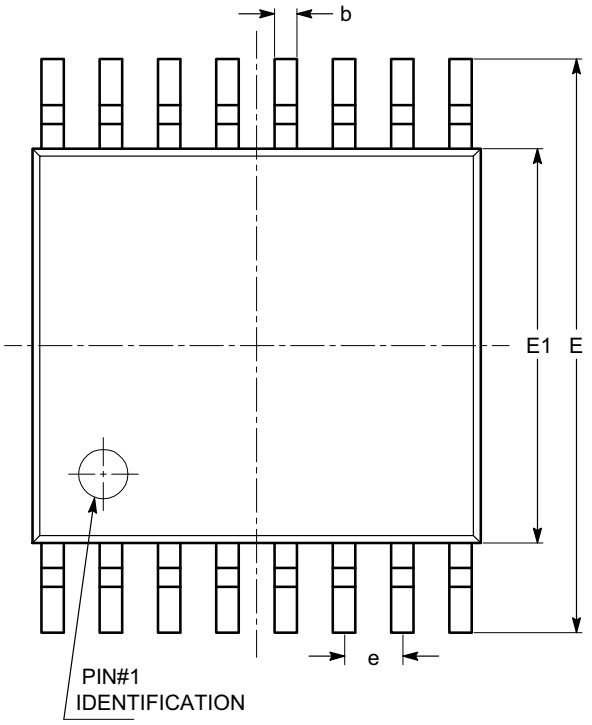


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

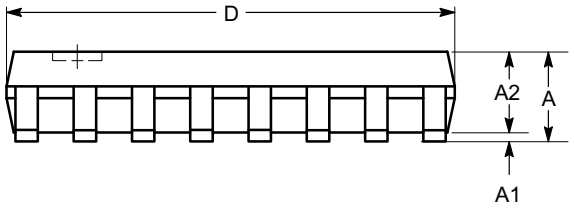
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN−01
ISSUE O

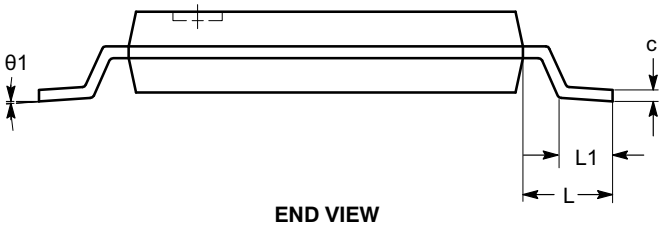


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Table 9. ORDERING INFORMATION

Part Number (Note 15)	**Marking** (Note 15)	**Package Type**	**Temperature**
PCS3P624Z0xyG−08−ST	3P624Z0xyG	8−pin 150−mil SOIC − TUBE, Green	Commercial
PCS3I624Z0xyG−08−ST	3I624Z0xyG	8−pin 150−mil SOIC − TUBE, Green	Industrial
PCS3P624Z0xyG−08−SR	3P624Z0xyG	8−pin 150−mil SOIC − TAPE & REEL, Green	Commercial
PCS3I624Z0xyG−08−SR	3I624Z0xyG	8−pin 150−mil SOIC − TAPE & REEL, Green	Industrial
PCS3P624Z0xyG−08−TT	3P624Z0xyG	8−pin 4.4−mm TSSOP − TUBE, Green	Commercial
PCS3I624Z00xyG−08−TT	3I624Z0xyG	8−pin 4.4−mm TSSOP − TUBE, Green	Industrial
PCS3P624Z0xyG−08−TR	3P624Z0xyG	8−pin 4.4−mm TSSOP − TAPE & REEL, Green	Commercial
PCS3I624Z0xyG−08−TR	3I624Z0xyG	8−pin 4.4−mm TSSOP − TAPE & REEL, Green	Industrial
PCS3P624Z0xyG−16−ST	3P624Z0xyG	16−pin 150−mil SOIC − TUBE, Green	Commercial
PCS3I624Z0xyG−16−ST	3I624Z0xyG	16−pin 150−mil SOIC − TUBE, Green	Industrial
PCS3P624Z0xyG−16−SR	3P624Z0xyG	16−pin 150−mil SOIC − TAPE & REEL, Green	Commercial
PCS3I624Z0xyG−16−SR	3I624Z0xyG	16−pin 150−mil SOIC − TAPE & REEL, Green	Industrial
PCS3P624Z0xyG−16−TT	3P624Z0xyG	16−pin 4.4−mm TSSOP − TUBE, Green	Commercial
PCS3I624Z0xyG−16−TT	3I624Z0xyG	16−pin 4.4−mm TSSOP − TUBE, Green	Industrial
PCS3P624Z0xyG−16−TR	3P624Z0xyG	16−pin 4.4−mm TSSOP − TAPE & REEL, Green	Commercial
PCS3I624Z0xyG−16−TR	3I624Z0xyG	16−pin 4.4−mm TSSOP − TAPE & REEL, Green	Industrial

15. x = 5 / 9; y = B / C

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