QUADRUPLE BILATERAL SWITCHES

The HEF4066B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition).

The HEF4066B is pin compatible with the HEF4016B but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range

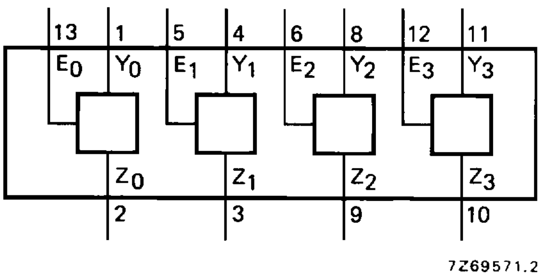


Fig. 1 Functional diagram.

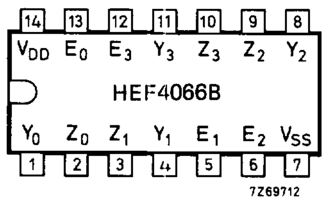


Fig. 2 Pinning diagram.

HEF4066BP(N): 14-lead DIL; plastic (SOT27-1)
HEF4066BD(F): 14-lead DIL; ceramic (cerdip) (SOT73))
HEF4066BT(D): 14-lead SO; plastic (SOT108-1)
( ): Package Designator North America

PINNING

E_0 to E_3 enable inputs

Y_0 to Y_3 input/output terminals

Z_0 to Z_3 input/output terminals

APPLICATION INFORMATION

An example of application for the HEF4066B is:

- Analogue and digital switching

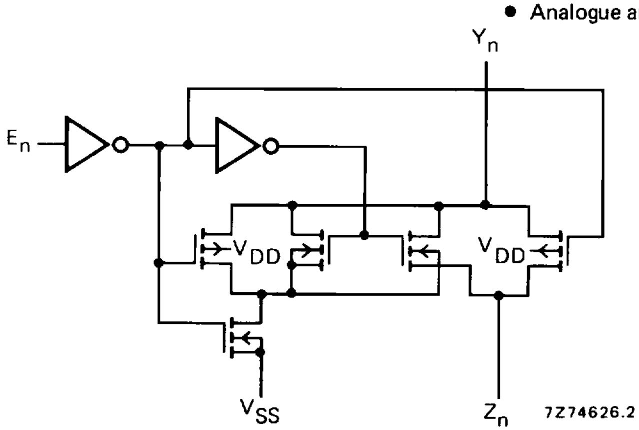


Fig. 3 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch P max. 100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V_{DD} V	symbol	min.	typ.	max.		conditions
ON resistance	5	R_{ON}	–	350	2500	Ω	E_n at V_{DD}; $V_{is} = V_{SS}$ to V_{DD}; see Fig. 4
	10		–	80	245	Ω	
	15		–	60	175	Ω	
ON resistance	5	R_{ON}	–	115	340	Ω	E_n at V_{DD}; $V_{is} = V_{SS}$; see Fig. 4
	10		–	50	160	Ω	
	15		–	40	115	Ω	
ON resistance	5	R_{ON}	–	120	365	Ω	E_n at V_{DD}; $V_{is} = V_{DD}$; see Fig. 4
	10		–	65	200	Ω	
	15		–	50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	–	25	–	Ω	E_n at V_{DD}; $V_{is} = V_{SS}$ to V_{DD}; see Fig. 4
	10		–	10	–	Ω	
	15		–	5	–	Ω	
OFF state leakage current, any channel OFF	5	I_{OZ}	–	–	–	nA	E_n at V_{SS}
	10		–	–	–	nA	
	15		–	–	200	nA	
E_n input voltage LOW	5	V_{IL}	–	2,25	1	V	I_{is} = 10 μA; see Fig. 9
	10		–	4,50	2	V	
	15		–	6,75	2	V	

	V_{DD} V	symbol	T_{amb} (°C) −40 max.	+25 max.	+85 max.		conditions
Quiescent device current	5	I_{DD}	1,0	1,0	7,5	μA	V_{SS} = 0; all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		2,0	2,0	15,0	μA	
	15		4,0	4,0	30,0	μA	
Input leakage current at E_n	15	$\pm I_{IN}$	–	300	1000	nA	E_n at V_{SS} or V_{DD}

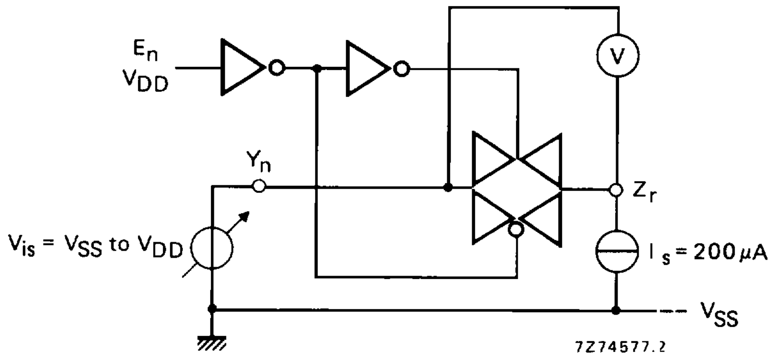


Fig. 4 Test set-up for measuring R_{ON}.

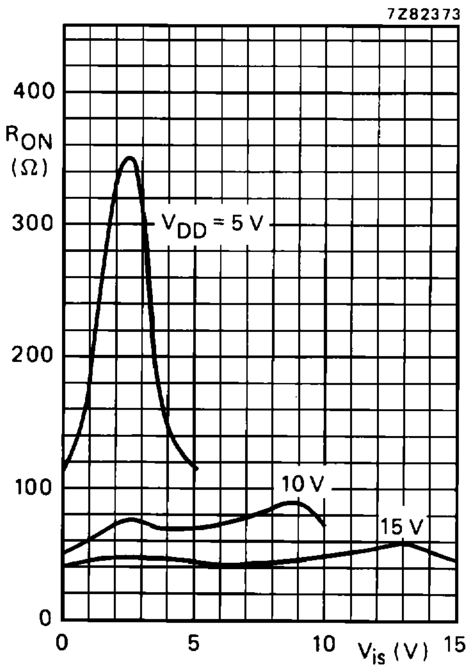


Fig. 5 Typical R_{ON} as a function of input voltage.

E_n at V_{DD}
I_{is} = 200 μA
V_{SS} = 0 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS}.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		10	20	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		10	20	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
Output disable times						
$E_n \rightarrow V_{os}$	5		80	160	ns	
HIGH	10	t_{PHZ}	65	130	ns	note 2
	15		60	120	ns	
	5		80	160	ns	
LOW	10	t_{PLZ}	70	140	ns	note 2
	15		70	140	ns	
Output enable times						
$E_n \rightarrow V_{os}$	5		40	80	ns	
HIGH	10	t_{PZH}	20	40	ns	note 2
	15		15	30	ns	
	5		45	90	ns	
LOW	10	t_{PZL}	20	40	ns	note 2
	15		15	30	ns	
Distortion, sine-wave	5		0,25		%	
response	10		0,04		%	note 3
	15		0,04		%	
Crosstalk between	5		–		MHz	
any two channels	10		1		MHz	note 4
	15		–		MHz	
Crosstalk; enable	5		–		mV	
input to output	10		50		mV	note 5
	15		–		mV	
OFF-state	5		–		MHz	
feed-through	10		1		MHz	note 6
	15		–		MHz	
ON-state frequency	5		–		MHz	
response	10		90		MHz	note 7
	15		–		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$800\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3\,500\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$10\,100\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; E_n = V_{DD}; V_{is} = V_{DD} (square-wave); see Figs 6 and 10.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; E_n = V_{DD} (square-wave);
   V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Figs 6 and 11.
3. R_L = 10 kΩ; C_L = 15 pF; E_n = V_{DD}; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   f_{is} = 1 kHz; see Fig. 7.
4. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB; E_n (A) = V_{SS}; E_n (B) = V_{DD}; see Fig. 8.
5. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; E_n = V_{DD} (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 6.
6. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{SS}; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 7.
7. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{DD}; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 7.

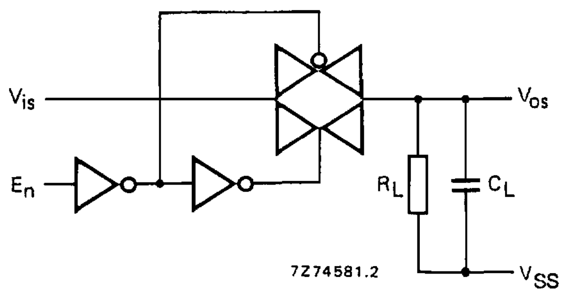


Fig. 6.

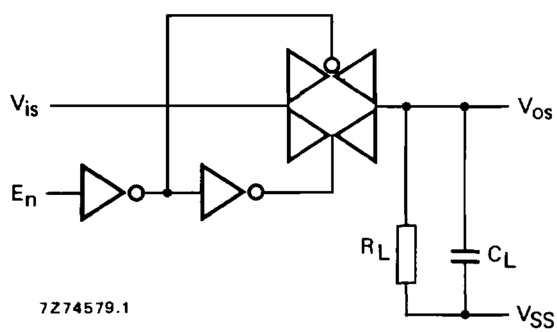


Fig. 7.

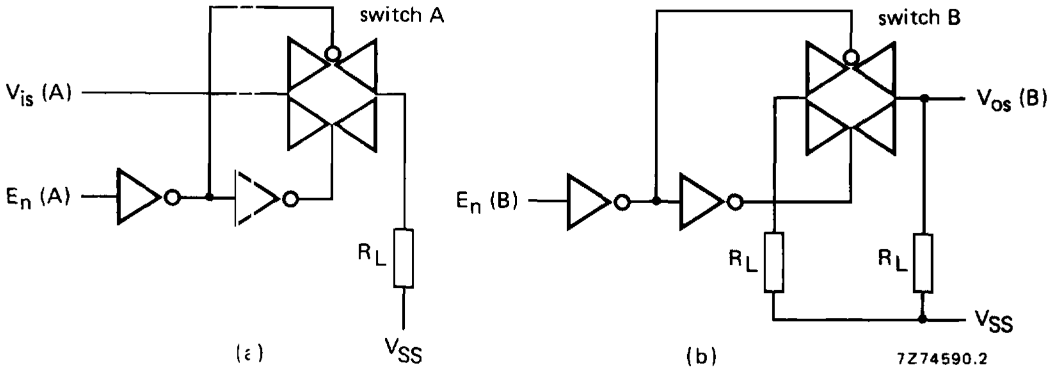

switch A
V_{is} (A)
E_n (A)
R_L
V_{SS}
(a)
switch B
V_{os} (B)
E_n (B)
R_L
R_L
V_{SS}
(b)
7Z74590.2

Fig. 8.

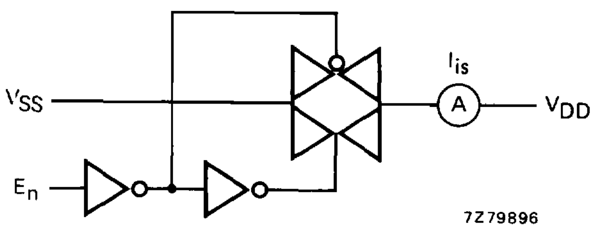

V_{SS}
I_{is}
A
V_{DD}
E_n
7Z79896

Fig. 9.

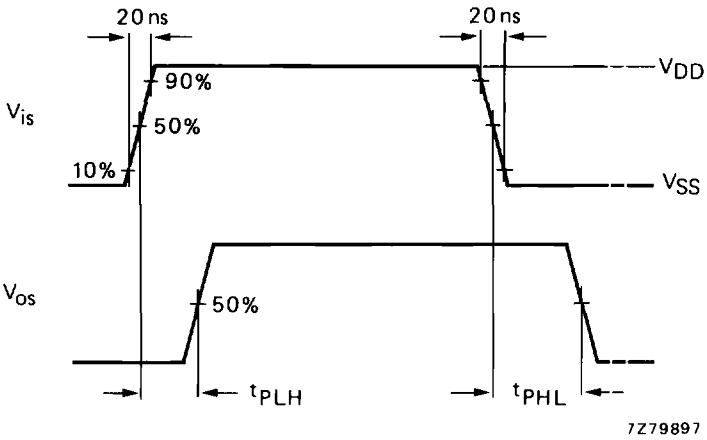
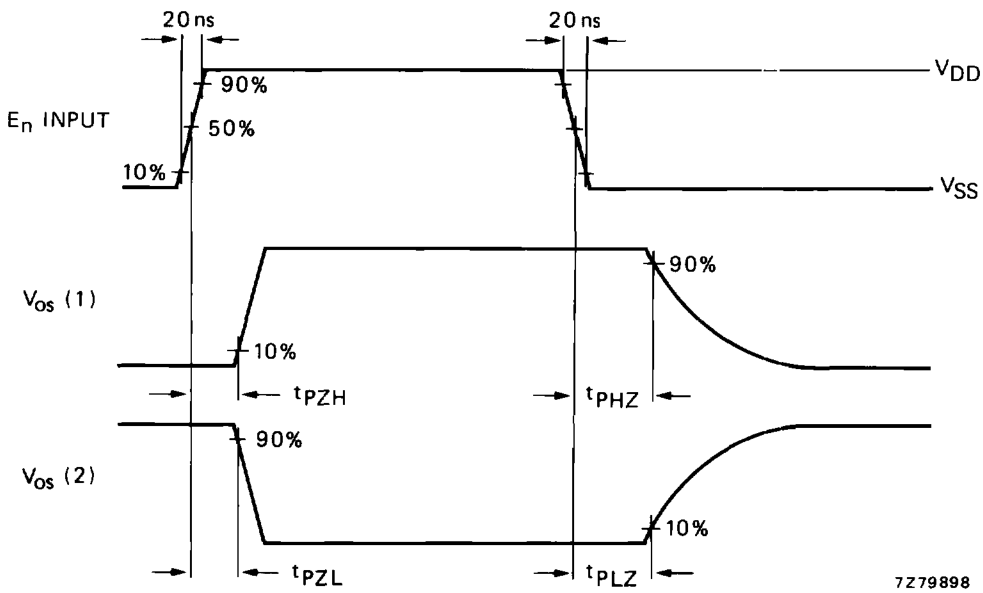


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os}.



(1) V_{is} at V_{DD}; (2) V_{is} at V_{SS}.

Fig. 11 Waveforms showing output disable and enable times.