SCLS107C - DECEMBER 1982 - REVISED MAY 1997

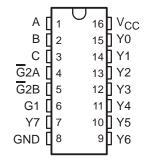
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Thin Shrink
 Small-Outline (PW), and Ceramic Flat (W)
 Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J)
 300-mil DIPs

description

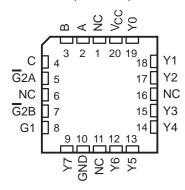
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SN54HC138 . . . J OR W PACKAGE SN74HC138 . . . D, N, OR PW PACKAGE (TOP VIEW)



SN54HC138...FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN54HC138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC138 is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

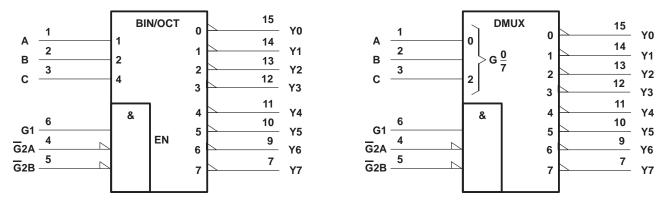


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FUNCTION TABLE

	INPUTS								OUTI	DUTE			
	ENABLE	<u> </u>		SELECT	•				0011	-013			
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
Х	X	Н	Х	X	X	Н	Н	Н	Н	Н	Н	Н	Н
L	X	X	Х	Χ	X	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
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Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

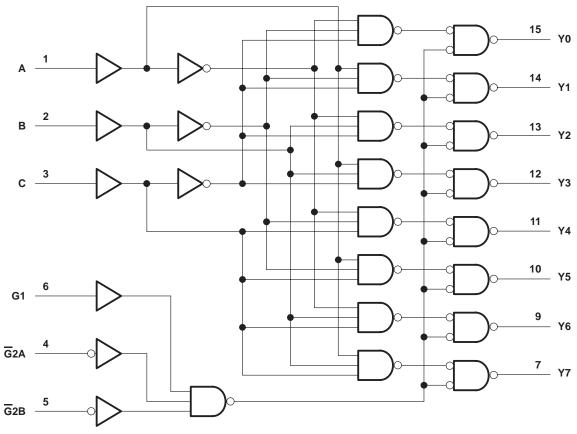
logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, PW, and W packages.



logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1) ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .	113°C/W
N package .	
PW package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



SN54HC138, SN74HC138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions

			SI	SN54HC138			SN74HC138		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 6 V	4.2			4.2			
		V _{CC} = 2 V	0		0.5	0		0.5	
V_{IL}	Low-level input voltage	V _{CC} = 4.5 V	0		1.35	0		1.35	V
		VCC = 6 V	0		1.8	0		1.8	
VI	Input voltage		0		VCC	0		VCC	V
VO	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V	0		1000	0		1000	
t _t	Input transition (rise and fall) time	V _{CC} = 4.5 V	0		500	0		500	ns
		V _{CC} = 6 V	0		400	0		400	
TA	Operating free-air temperature		-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CO	V	Т	A = 25°C	;	SN54H	C138	SN74HC138		UNIT	
PARAMETER	l lESI CC	ONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT
			2 V	1.9	1.998		1.9		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
Voн	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
	VI = VIH or VIL		2 V		0.002	0.1		0.1		0.1	V
		I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
VOL			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
Icc	$V_I = V_{CC}$ or 0,	I _O = 0	6 V			8		160		80	μΑ
C _i			2 V to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Vaa	T,	ղ = 25°C	;	SN54F	IC138	SN74HC138		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT	
		Any Y	2 V		67	180		270		225		
	A, B, or C		4.5 V		18	36		54		45		
			6 V		15	31		46		38	ns	
^t pd			2 V		66	155		235		195		
	Enable	Any Y	4.5 V		18	31		47		39		
			6 V		15	26		40		33		
			2 V		38	75		110		95		
t _t		Any	Any 4.5 V 8 15 22					19	ns			
			6 V		6	13		19		16		

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	85	pF

PARAMETER MEASUREMENT INFORMATION **VCC** From Output Test Input 50% 50% **Under Test Point** $C_L = 50 pF$ - tPHL (see Note A) ۷он In-Phase 90% 50% Output 10% V_{OL} **LOAD CIRCUIT** 10% - tPHL Vон 90% 90% Input 90% **Out-of-Phase** Output **VOLTAGE WAVEFORM VOLTAGE WAVEFORMS INPUT RISE AND FALL TIMES** PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_f = 6 ns.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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PRICING/AVAILABILITY | APPLICATION NOTES |
RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

SN54HC138, 3-Line To 8-Line Decoders/Demultiplexers

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54HC138			
Voltage Nodes (V)	6, 5, 2			
Vcc range (V)	2.0 to 6.0			
Input Level	CMOS			
Output Level	CMOS			
Output	2S			
From	3			
То	8			

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DESCRIPTION<u>Back to Top</u>

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- Implications of Slow or Floating CMOS Inputs (SCBA004C Updated: 02/01/1998)
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- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB Updated: 07/28/2000)
- More Power In Less Space Technical Article (SCAU001A, 850 KB Updated: 03/01/1996)

PRICING/AVAILABILITY

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ORDERABLE DEVICE	<u>PACKAGE</u>	<u>PINS</u>	TEMP (°C)	<u>STATUS</u>	BUDGETARY PRICE US\$/UNIT OTY=1000+	PACK QTY	<u>DSCC</u> NUMBER	PRICING/AVAILABILITY
JM38510/65802B2A	<u>FK</u>	20	-55 TO 125	ACTIVE	11.15	1		Check stock or order
JM38510/65802BEA	Ī	16	-55 TO 125	ACTIVE	6.38	1		Check stock or order
JM38510/65802BFA	<u>W</u>	16	-55 TO	ACTIVE	11.44	150		Check stock or order

			125					
SN54HC138J	J	16	-55 TO 125	ACTIVE	1.10	1		Check stock or order
SNJ54HC138FK	<u>FK</u>	20	-55 TO 125	ACTIVE	8.65	1	84062012A	Check stock or order
SNJ54HC138J	Ī	16	-55 TO 125	ACTIVE	1.79	1		Check stock or order
SNJ54HC138W	W	16	-55 TO 125	ACTIVE	9.30	1	8406201FA	Check stock or order

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SN74HC138D	<u>D</u>	16	-40 TO 85	ACTIVE	0.35	40	Check stock or order
SN74HC138DBR	<u>DB</u>	16	-40 TO 85	ACTIVE	0.35	2000	Check stock or order
SN74HC138DR	<u>D</u>	16	-40 TO 85	ACTIVE	0.38	2500	Check stock or order

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SN74HC138N	<u>N</u>	16	-40 TO 85	ACTIVE	0.33	25	Check stock or order
SN74HC138N3	N	16	-40 TO 85	OBSOLETE			
SN74HC138NSR	<u>NS</u>	16	-40 TO 85	ACTIVE	0.43	2000	Check stock or order
SN74HC138PWLE	<u>PW</u>	16	-40 TO 85	OBSOLETE			
SN74HC138PWR	<u>PW</u>	16	-40 TO 85	ACTIVE	0.35	2000	Check stock or order

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