

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# RD74LVC273B

## Octal D-type Flip-Flops with Clear

REJ03D0323-0100Z

Rev.1.00

Jun. 16, 2004

### Description

The RD74LVC273B has eight edge trigger D-type flip-flops with clear in a 20-pin package. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state. Low-voltage and high-speed operation is suitable for battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC} = 1.65\text{ V to }5.5\text{ V}$
- All inputs  $V_{IH}(\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V to }5.5\text{ V})$
- All outputs  $V_{OUT}(\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V})$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- High Output current
  - $\pm 4\text{ mA} (@V_{CC} = 1.65\text{ V})$
  - $\pm 8\text{ mA} (@V_{CC} = 2.3\text{ V})$
  - $\pm 12\text{ mA} (@V_{CC} = 2.7\text{ V})$
  - $\pm 24\text{ mA} (@V_{CC} = 3.0\text{ V to }5.5\text{ V})$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RD74LVC273BFPEL	SOP-20 pin(JEITA)	FP-20DAV	FP	EL (2,000 pcs / reel)
RD74LVC273BTELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs / reel)

### Function Table

$\overline{\text{CLR}}$	Inputs		Output Q
	CLK	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	$\downarrow$	X	$Q_0$

Note: H: High level

L: Low level

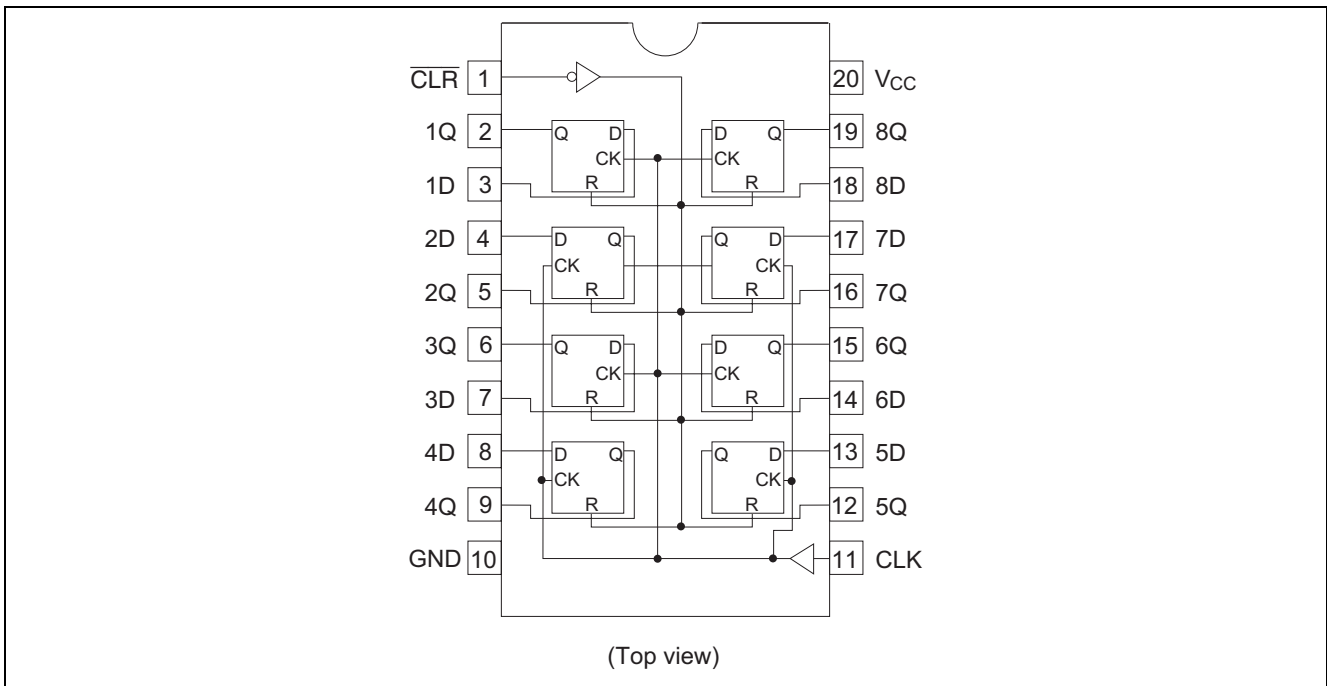
X: Immaterial

$\uparrow$ : Low to high transition

$\downarrow$ : High to low transition

$Q_0$ : Output level before the indicated steady state input conditions were established.

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 7.0	V	
Input diode current	$I_{IK}$	-50	mA	$V_I = -0.5$ V
Input voltage	$V_I$	-0.5 to 7.0	V	
Output diode current	$I_{OK}$	-50	mA	$V_O = -0.5$ V
		50		$V_O = V_{CC} + 0.5$ V
Output voltage	$V_O$	-0.5 to $V_{CC} + 0.5$	V	Output "H" or "L"
		-0.5 to 7.0		$V_{CC}$ : OFF
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	100	mA	
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}$ C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	1.5 to 5.5	V	Data hold
		1.65 to 5.5		At operation
Input/Output voltage	$V_I$	0 to 5.5	V	CLK, $\overline{CLR}$ , D
	$V_O$	0 to $V_{CC}$		Output "H" or "L"
		0 to 5.5		$V_{CC}$ : OFF
Operating temperature	$T_a$	-40 to 85	°C	
Output current	$I_{OH}$	-4	mA	$V_{CC} = 1.65\text{ V}$
		-8		$V_{CC} = 2.3\text{ V}$
		-12		$V_{CC} = 2.7\text{ V}$
		-24		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
	$I_{OL}$	4	mA	$V_{CC} = 1.65\text{ V}$
		8		$V_{CC} = 2.3\text{ V}$
		12		$V_{CC} = 2.7\text{ V}$
		24		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
Input rise / fall time* <sup>1</sup>	$t_r / t_f$	20	ns/V	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$
		10		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.  
Waveform: Refer to test circuit of switching characteristics.

## Electrical Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V <sub>IH</sub>	1.65 to 1.95	V <sub>CC</sub> × 0.65	—	V	
		2.3 to 2.7	1.7	—		
		2.7 to 3.6	2.0	—		
		4.5 to 5.5	V <sub>CC</sub> × 0.7	—		
	V <sub>IL</sub>	1.65 to 1.95	—	V <sub>CC</sub> × 0.35		
		2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
		4.5 to 5.5	—	V <sub>CC</sub> × 0.3		
Output voltage	V <sub>OH</sub>	1.65 to 5.5	V <sub>CC</sub> - 0.2	—	V	I <sub>OH</sub> = -100 μA
		1.65	1.2	—		I <sub>OH</sub> = -4 mA
		2.3	1.7	—		I <sub>OH</sub> = -8 mA
		2.7	2.2	—		I <sub>OH</sub> = -12 mA
		3.0	2.4	—		
		3.0	2.2	—		I <sub>OH</sub> = -24 mA
		4.5	3.8	—		
	V <sub>OL</sub>	1.65 to 5.5	—	0.2		I <sub>OL</sub> = 100 μA
		1.65	—	0.45		I <sub>OL</sub> = 4 mA
		2.3	—	0.7		I <sub>OL</sub> = 8 mA
		2.7	—	0.4		I <sub>OL</sub> = 12 mA
		3.0	—	0.55		I <sub>OL</sub> = 24 mA
		4.5	—	0.55		
Input current	I <sub>IN</sub>	0 to 5.5	—	±5.0	μA	V <sub>IN</sub> = 5.5 V or GND
Output leak current	I <sub>OFF</sub>	0	—	±5.0	μA	V <sub>IN</sub> /V <sub>OUT</sub> = 5.5 V
Quiescent supply current	I <sub>CC</sub>	2.7 to 3.6	—	±5.0	μA	V <sub>IN</sub> = 3.6 V to 5.5 V
		2.7 to 5.5	—	5.0		V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	2.7 to 3.6	—	500		V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6)V, other inputs at V <sub>CC</sub> or GND

## Switching Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C			Unit	FROM (Input)	TO (Output)
			Min	Typ	Max			
Maximum clock frequency	f <sub>max</sub>	1.8±0.15	—	—	55.0	MHz		
		2.5±0.2	—	—	95.0			
		2.7	—	—	150.0			
		3.3±0.3	—	—	150.0			
		5.0±0.5	—	—	150.0			
Propagation delay time	t <sub>PLH</sub>	1.8±0.15	1.0	—	21.6	ns	CLK	Q
		2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.5			
		3.3±0.3	1.5	—	7.5			
		5.0±0.5	1.0	—	6.0			
	t <sub>PHL</sub>	1.8±0.15	1.0	—	21.6	ns	CLR	Q
		2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.5			
		3.3±0.3	2.0	—	7.5			
		5.0±0.5	1.0	—	6.0			
Setup time	t <sub>SU</sub>	1.8±0.15	6.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	2.0	—	—			
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t <sub>H</sub>	1.8±0.15	4.0	—	—	ns		
		2.5±0.2	2.0	—	—			
		2.7	1.5	—	—			
		3.3±0.3	1.5	—	—			
		5.0±0.5	1.5	—	—			
Pulse width	t <sub>W</sub>	1.8±0.15	9.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
		5.0±0.5	3.3	—	—			
Between output pins skew*1	t <sub>OSLH</sub> t <sub>OSHL</sub>	1.8±0.15	—	—	—	ns		
		2.5±0.2	—	—	—			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C <sub>IN</sub>	3.3	—	4.0	—	pF		
Output capacitance	C <sub>O</sub>	3.3	—	8.0	—	pF		

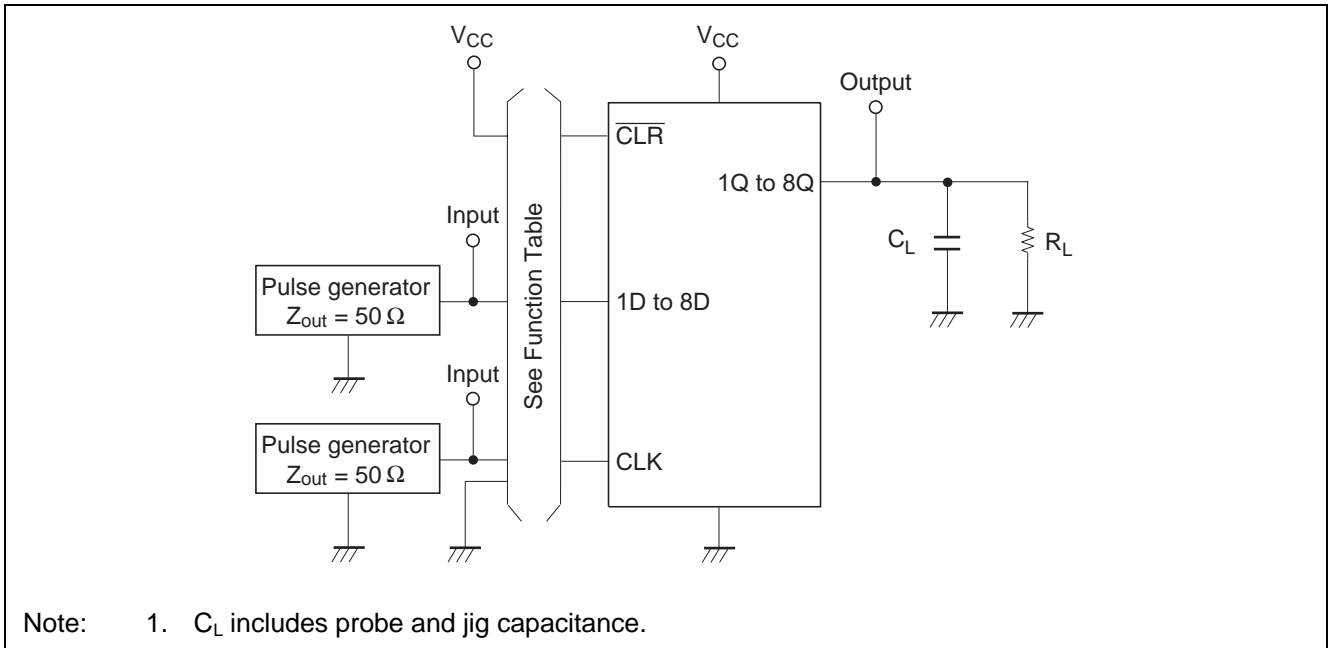
Note: 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

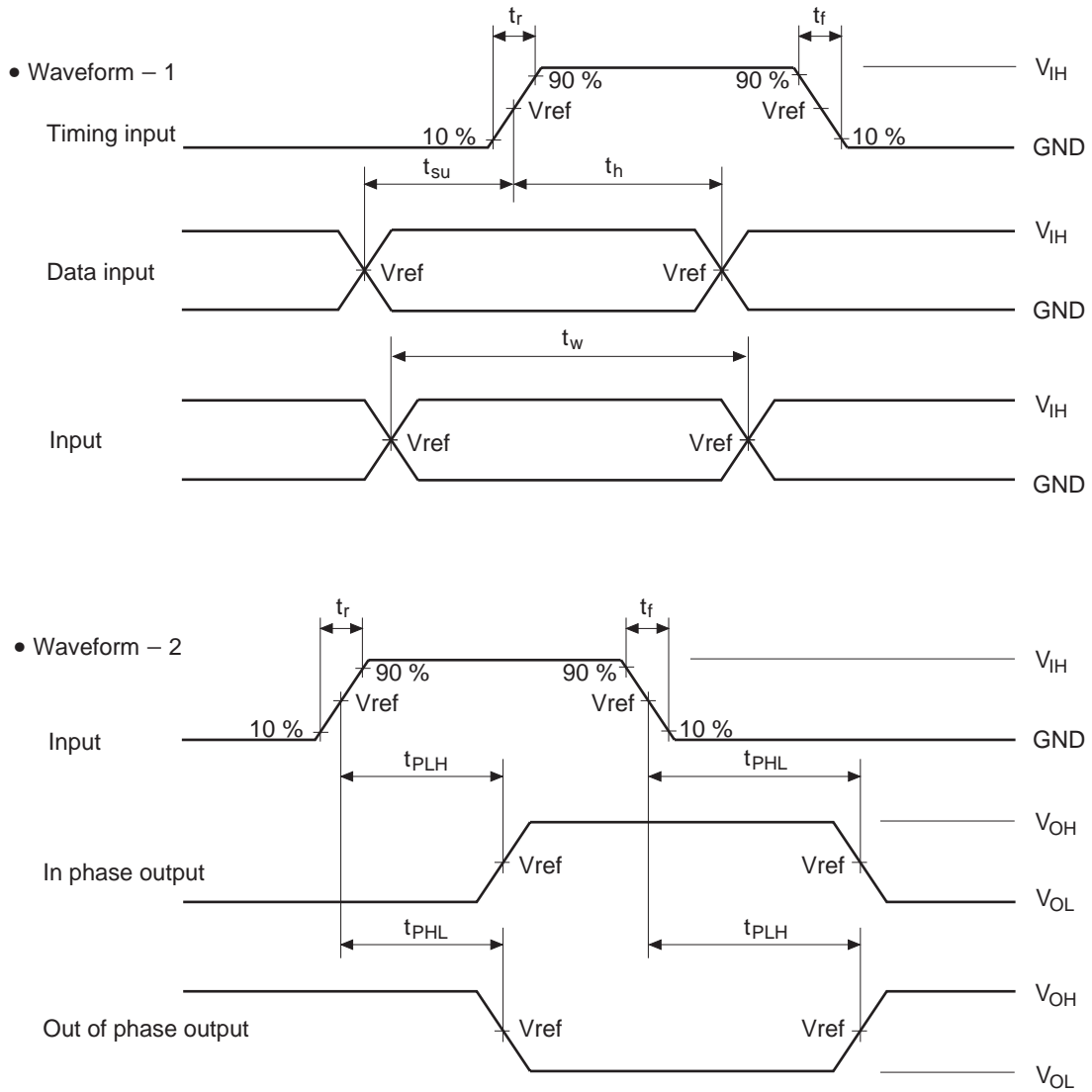
## Operating Characteristics

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^{\circ}C$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	$C_{PD}$	1.8	—	25	—	pF	$f = 10 \text{ MHz}$
		2.5	—	26	—		
		3.3	—	28	—		
		5.0	—	32	—		

## Test Circuit



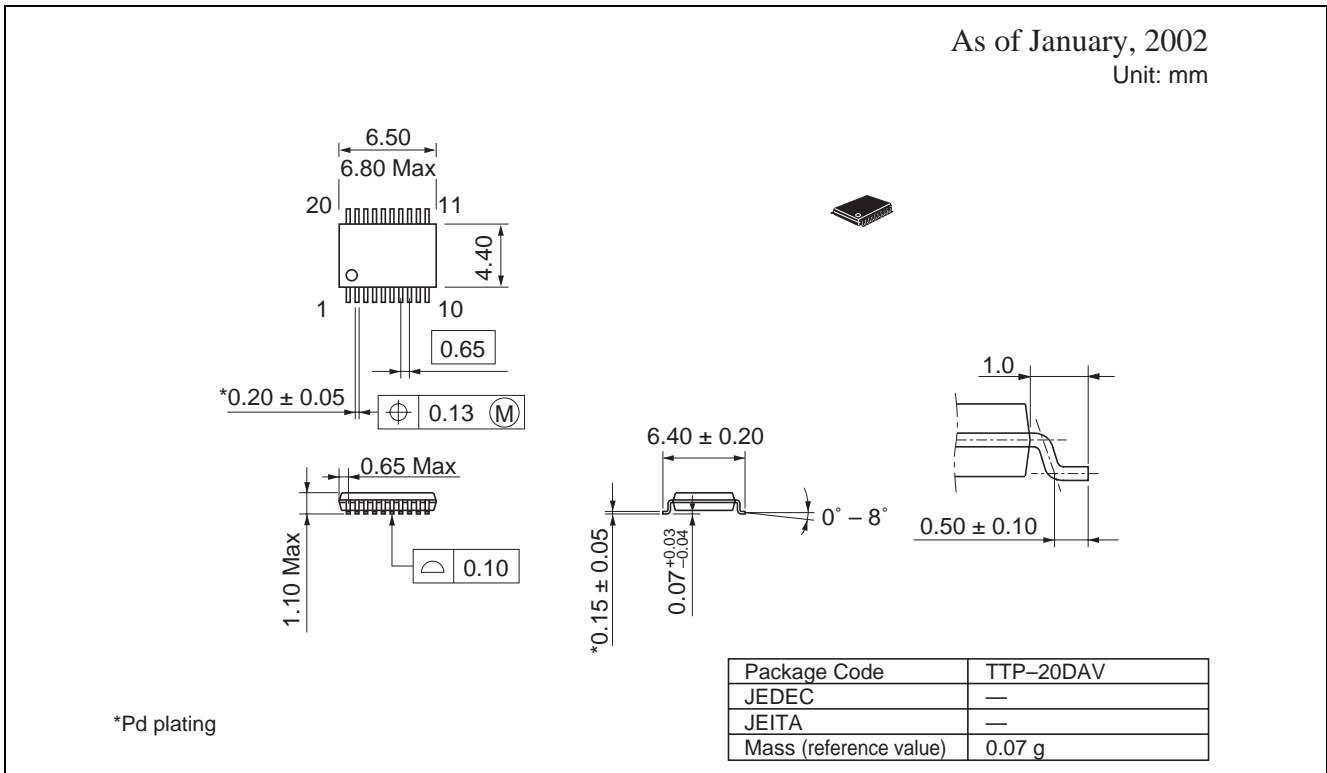
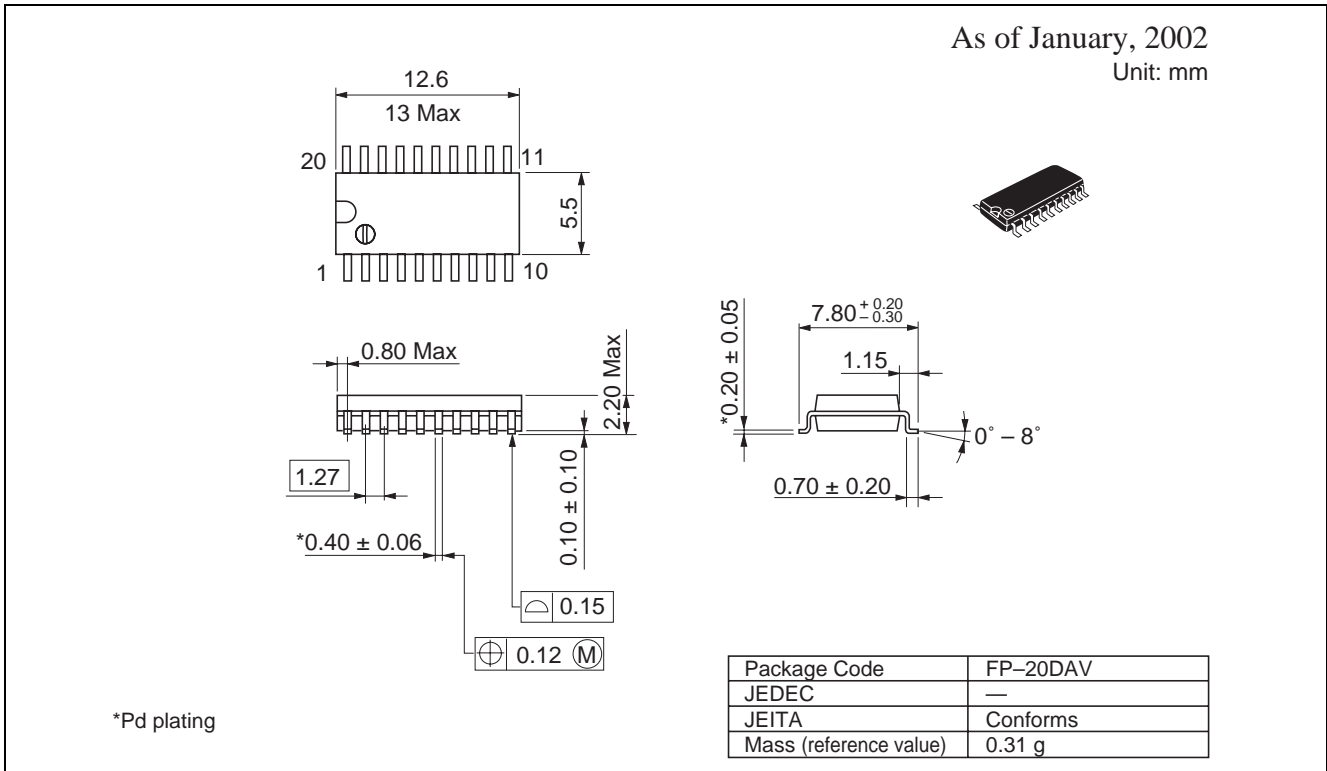




Vcc (V)	INPUTS		Vref	CL	RL
	V <sub>IH</sub>	t <sub>r</sub> / t <sub>f</sub>			
Vcc = 1.8±0.15 V	Vcc	≤ 2 ns	1/2 Vcc	30 pF	1.0 kΩ
Vcc = 2.5±0.2 V	Vcc	≤ 2 ns	1/2 Vcc	30 pF	500 Ω
Vcc = 2.7 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
Vcc = 3.3±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
Vcc = 5.0±0.5 V	Vcc	≤ 2.5 ns	1/2 Vcc	50 pF	500 Ω

Notes: 1. Input waveform: PRR ≤ 10 MHz, duty cycle 50%.  
 2. The output is measured one at a time with one transition per measurement.

Package Dimensions



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