REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R031-97.	96-11-06	R. MONNIN
B	Add device class T criteria. Editorial changes throughout. Redrawn. -lgt	98-12-23	R. MONNIN
C	Add vendor CAGE F8859. Updated footnote 2/ in table I to accommodate RHA designator "D". Update boilerplate to reflect current requirements. -rrp	02-11-27	R. MONNIN

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
95-07-13

REVISION LEVEL
C

MICROCIRCUIT, LINEAR, RADIATION HARDENED, CMOS, QUAD DIFFERENTIAL, LINE DRIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95632**

SHEET 1 OF 23

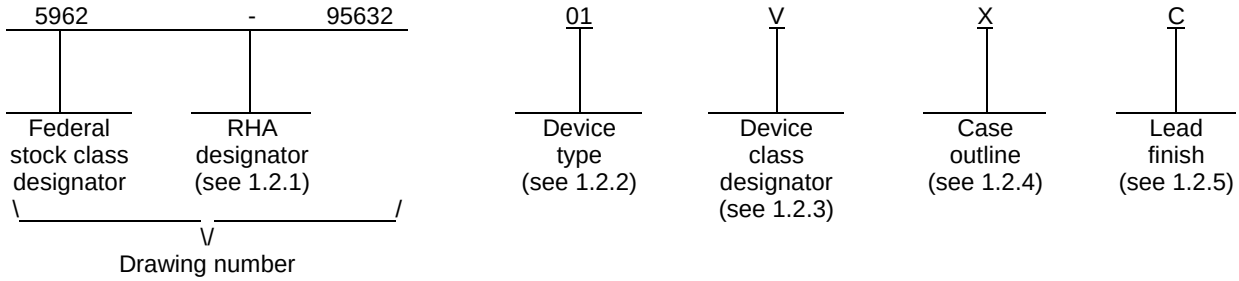
DSCC FORM 2233
APR 97

5962-E054-03

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	26CT31RH	Radiation hardened quad differential line driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage	-0.5 V to +7.0 V
Inputs, E, $\overline{E}$ voltage	-0.5 V to V_{DD}+0.5 V
Output voltage (power on or off (0.0 V))	-0.5 V to +7.0 V
DC diode input current (any input)	±20 mA
DC drain current (any output)	350 mA
DC V_{DD} or ground current	400 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Dip package	75°C C/W
Flatpack package	95°C C/W
Power dissipation at T_A = 125°C (P_D)	0.44 W 2/
For T_A = -55°C to 125°C:	
Dip package	.667 W
Flatpack package	.526 W

1.4 Recommended operating conditions.

Operating temperature range (T_A)	-55°C to +125°C
Supply voltage range (V_{DD})	+4.5 V to +5.5 V
Low input voltage (V_{IL})	0 V to 0.8 V, maximum
High input voltage (V_{IH})	V_{DD} to V_{DD}/2 V, minimum
Input rise and fall time	500 ns maximum
Dynamic current (I_{DYN}) at +25 °C	3 mA
Power dissipation capacitance (CP_D) at +25°C	170 pF

1.5 Radiation features

SEP effective LET 3/	> 100 (MEV/mg/cm^2)
Neutron 3/	> 1 x 10^{14} neutrons/cm^2
Dose rate upset 3/	> 5 x 10^8 Rads (Si)/sec
Dose rate survivability 3/	> 5 x 10^{11} Rads (Si)/sec
Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):	
Device classes M, Q, or V	3 x 10^5 Rads (Si)
Device class T	1 x 10^5 Rads (Si)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum device power dissipation is defined as V_{DD} x I_{CC} and must withstand the added P_D due to output current test I_O at T_A = +125°C.
3/ Guaranteed by process or design, not tested.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 4.5 V and 5.5 V, I_O = -20 mA 3/ 4/	1, 2, 3	01	2.5		V
Low level output voltage	V_{OL}	V_{DD} = 4.5 V and 5.5 V, I_O = 20 mA 3/ 4/	1, 2, 3	01		0.5	V
Differential output voltage	V_T, $\overline{V_T}$	$V_{DD} = V_{IH}$ = 4.5 V, V_{IL} = 0 V, R_L = R1 + R2 5/	1, 2, 3	01	2.0		V
Difference in differential output	$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	$V_{DD} = V_{IH}$ = 4.5 V, V_{IL} = 0 V, R_L = R1 + R2 5/	1, 2, 3	01		0.4	V
Common Mode Output voltage	$\lvert V_{OS} - \overline{V_{OS}} \rvert$	$V_{DD} = V_{IH}$ = 4.5 V, V_{IL} = 0 V, R_L = R1 + R2 5/	1, 2, 3	01		3.0	V
Difference in Common Mode Output	$\lvert V_{OS} - \overline{V_{OS}} \rvert$	$V_{DD} = V_{IH}$ = 4.5 V, V_{IL} = 0 V, R_L = R1 + R2 5/	1, 2, 3	01		0.4	V
High level input voltage	V_{IH}	V_{DD} = 4.5 V, 5.5 V 6/	1, 2, 3	01	V_{DD}/2.0		V
Low level input voltage	V_{IL}	V_{DD} = 4.5 V, 5.5 V 6/	1, 2, 3	01		0.8	V
Standby supply current	I_{DDSB}	V_{DD} = 5.5 V, Output = open, $V_{IN} = V_{DD}$ or GND	1, 2, 3	01		500	µA
Three-state output leakage current	I_{OZ}	V_{DD} = 5.5 V, Force voltages = 0 V or V_{DD} 7/	1, 2, 3	01		±5.0	µA
Delta Supply current	ΔI_{CC}	V_{DD} = 5.5 V, V_{IN} = 2.4 V, 0.5 V	1, 2, 3	01		2.0	mA
Input leakage	I_{IN}	V_{DD} = 5.5 V, $V_{IN} = V_{DD}$ or GND	1, 2, 3	01		±1.0	µA
Output leakage current power off	I_{OFF}	V_{DD} = 0.0 V, V_{OUT} = 6.0 V, -250 mV, Inputs = GND	1, 2, 3	01	-100	100	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IC}	at -1.0 mA	1, 2, 3	01		-1.5	V
		at +1.0 mA				+1.5	
Functional test		See 4.4.1b	7, 8A, 8B	01			
Propagation delay time	T_{PLH}, T_{PHL}	V_{DD} = 4.5 V 5/	9, 10 ,11	01	2	22	ns
	T_{PZH}, T_{PZL}				5	28	
	T_{PLZ}, T_{PHZ}				2	22	
Rise and Fall time	T_{THL}, T_{TLH}	V_{DD} = 4.5 V 5/	9, 10, 11	01	1	10	ns
Output skew	T_{SKEW} 8/	V_{DD} = 4.5 V 5/ R_L = 100 Ω, C_L = 40 pF	9, 10, 11	01		3	ns
Note : The below parameters are not part of the Post Irradiation electrical performance characteristics. 9/							
Input capacitance	C_{IN}	V_{DD} = open, f = 1 MHz	4	01		12	pF
Output capacitance	C_{OUT}	V_{DD} = open, f = 1 MHz	4	01		12	pF
Operating short circuit	I_{OS}	V_{DD} = 5.5 V, V_{IN} = V_{DD} or GND, V_{OUT} = 0 V 10/	1, 2, 3	01	-30	-150	mA
On-state resistance	R_{ON}	V_{DD} = 4.5 V, V_{OUT} = 1.5 V, V_{IN} = V_{DD} or GND	1, 2, 3	01		10	Ω

1/ Devices supplied to this drawing meet all levels M, D, P, L, R and F of irradiation for classes M, Q, or V and levels M, D, P, L, and R for class T. However, device classes M, Q, and V are only tested at the F or D levels depending upon the manufacturers, and class T is only tested at the R level (see paragraph 1.5). Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ All voltages referenced to device ground.
3/ Force/measure functions may be interchanged.
4/ V_{IL} = 0.8 V and V_{IN} = V_{CC}/2.
5/ These conditions are detailed in EIA specification RS-422, (R1 = R2 = 500 Ω). See figure 3 as applicable.
6/ This parameter tested as inputs for the V_{OL}, V_{OH}, and I_{OZ}, and function tests.
7/ The inputs are conditioned to have the output in the opposite state of the forcing I_{OZ} condition.
8/ Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
9/ Tested initially and after any design or process changes that affect these parameters, and therefore shall meet the values listed in table I.
10/ Only one output at a time shall be shorted.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 77 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein.

For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer’s QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer’s QM plan.

For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device class T, screening shall be in accordance with the device manufacturer’s Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

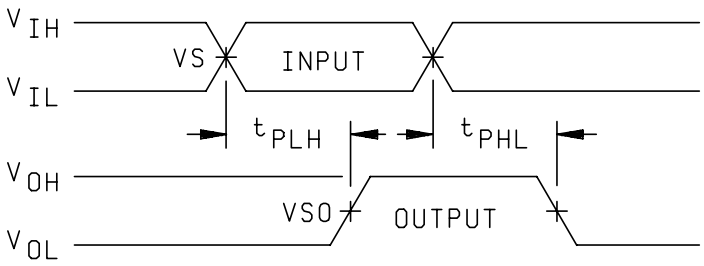
Device type	01
Case outline	E and X
Terminal number	Terminal symbol
1	A_{IN}
2	AO
3	$\overline{AO}$
4	ENABLE
5	$\overline{BO}$
6	BO
7	B_{IN}
8	GND
9	C_{IN}
10	CO
11	$\overline{CO}$
12	$\overline{ENABLE}$
13	$\overline{DO}$
14	DO
15	D_{IN}
16	V_{DD}

FIGURE 1. Terminal connections.

Device Power ON/OFF	INPUTS			OUTPUT	
	ENABLE	ENABLE	IN	OUT	$\overline{\text{OUT}}$
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF (0 V)	X	X	X	HI-Z	HI-Z

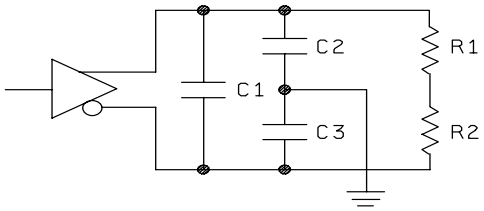
FIGURE 2. Truth table.

Propagation Delay Timing Diagram



Note : Voltage Levels
V_{DD} = 4.50 V
V_{IH} = 3.00 V
V_S = 1.30 V
V_{IL} = 0.0 V
GND = 0.0 V
V_{SO} = 50%

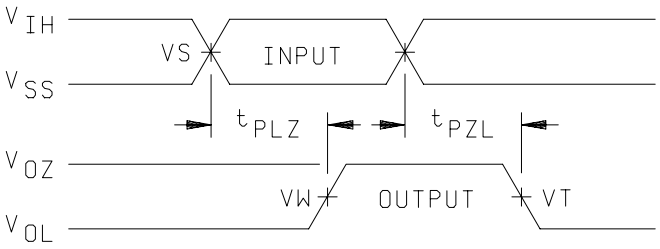
Propagation Delay Load Circuit



C1 = C2 = C3 = 40 pF
R1 = R2 = 50 Ω

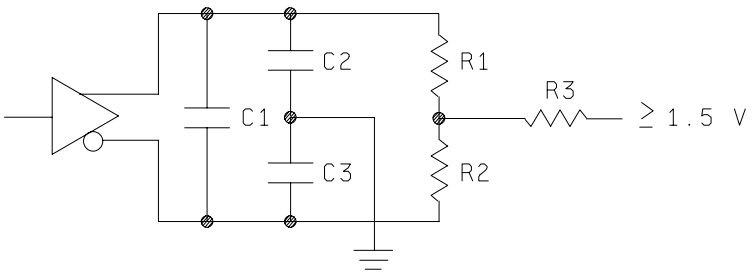
FIGURE 3. Timing and load circuit diagrams.

Three-state Low Timing Diagram



Note : Voltage Levels
V_{DD} = 4.50 V
V_{IH} = 3.00 V
V_S = 1.30 V
V_W = V_{OL} + 0.3 V
V_T = 0.60 V

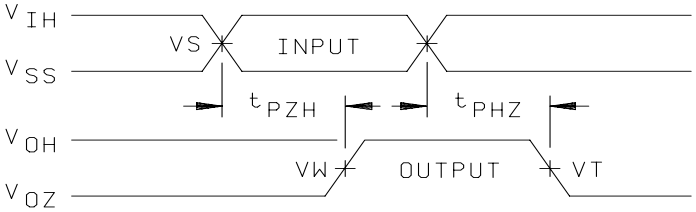
Three-state Low Load Circuit



C1 = C2 = C3 = 40 pF
R1 = R2 = 50 Ω
R3 = 500 Ω

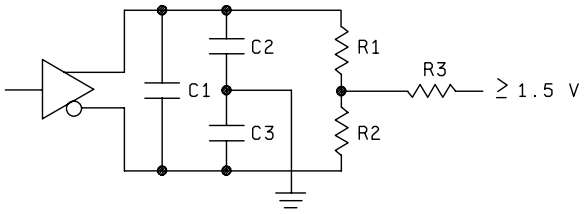
FIGURE 3. Timing and load circuit diagrams – Continued.

Three-state High Timing Diagram



Note : Voltage Levels
V_{DD} = 4.50 V
V_{IH} = 3.00 V
V_S = 1.30 V
V_T = V_{OH} -0.3 V
V_W = 2.00 V

Three-state High Load Circuit



C1 = C2 = C3 = 40 pF
R1 = R2 = 50 Ω
R3 = 500 Ω

FIGURE 3. Timing and load circuit diagrams – Continued.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,7,8A,8B, 9, 10,11 1/	1,2,3,7,8A,8B, 9,10,11 1/	1,2,3,7,8A,8B 9,10,11 1/ 2/	
Group A test requirements (see 4.4)	1,2,3,4,7,8A,8B, 9,10,11 3/	1,2,3,4,7,8A,8B, 9,10,11 3/	1,2,3,4,7,8A, 8B,9,10,11 3/	
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8A,8B,9, 10,11	1,2,3,7,8A,8B,9, 10,11	1,2,3,7,8A,8B 9,10,11 2/	
Group D end-point electrical parameters (see 4.4)	1	1, 7, 9	1, 7, 9	
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	

1/ PDA applies to subgroups 1, 7, and 9. For class V to subgroups 1, 7, 9, and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table I).
3/ Subgroup 4, if not tested, shall be guaranteed to the limits specified in table I.

TABLE IIB. Burn-in delta parameters and group C delta parameters at T_A = +25°C

TEST 1/	Device types
	ALL
I_{DDSB}	±100 µA
I_{OZ}	±1.0 µA
V_{OL}	±60 mV
V_{OH}	±150 mV
I_{IN}	±150 nA

1/ The above parameters shall be recorded before and after the required burn-in and life test to determine the delta.

TABLE III. Irradiation test connections .

(T_A = +25°C ±5°C; V_{DD} = 5.0 V ±10%)

TEST	OPEN	GROUND	VDD	½ VDD	50 kHz	25 kHz
Radiation Exposure	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16			

Note : Each pin except for V_{DD} and Ground will have a 47 kΩ resistor ±5%.

4.2.2 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535, or as specified in the QM plan, including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. Subgroup 4 (C_{IN} and C_{OUT}) should be measured only for initial qualification and after any process or design changes which may affect input or output capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein or as modified in the QM plan.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535.

4.4.4.2.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. Dose rate upset testing shall be performed on a technology process, in accordance with test method 1023 of MIL-STD-883 and herein (see 1.5 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the device. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract SEP testing shall be required on class Q, T and V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When applicable a copy of the following additional data shall be maintained and available from the device manufacturer:

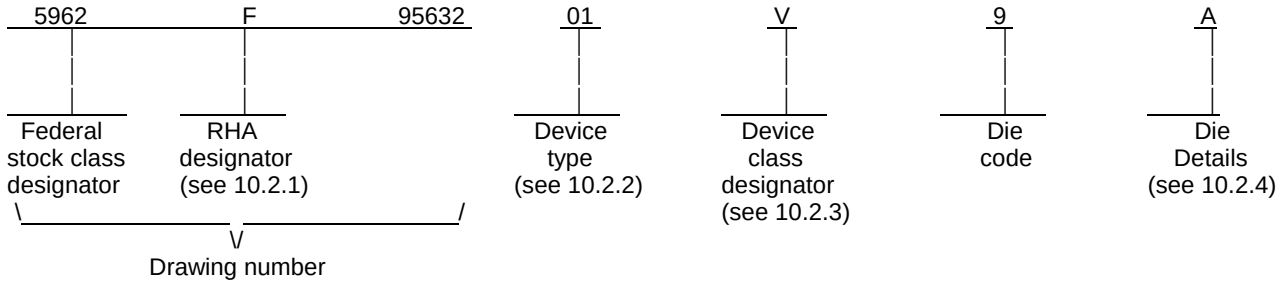
a. RHA upset levels.
b. Test conditions (SEP).
c. Number of upsets (SEP).
d. Number of transients (SEP).
e. Occurrence of latchup (SEP).

APPENDIX A
APPENDIX A FORMS PART OF SMD 5962-95632

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-26CT31RH	Radiation hardened quad differential line driver

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

10.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

10.2.4.3. Interface materials.

Die type	Figure number
01	A-1

10.2.4.4. Assembly related information.

Die type	Figure number
01	A-1

10.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standard, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3. of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.4. of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

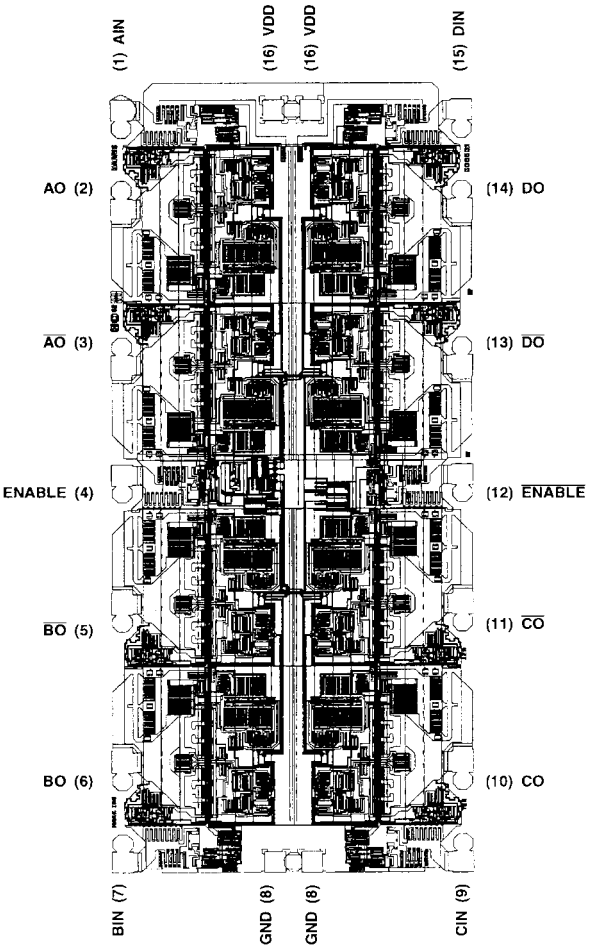
60 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines E and X (see Figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.
Die size: 2450 x 4950 microns
Die thickness: 21 ± 1 mils

Interface materials.
Top metallization: Si Al Cu 10.0 kÅ± 2 kÅ
Backside metallization: None: chemical etch

Glassivation.
Type: PSG
Thickness: 8 kÅ ± 1 kÅ

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: substrate internally tied to V_{DD}
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-11-27

Approved sources of supply for SMD 5962-95632 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962D9563201QXA	F8859	26CT31K02Q
5962D9563201VXA	F8859	26CT31K02V
5962D9563201QXC	F8859	26CT31K01Q
5962D9563201VXC	F8859	26CT31K01V
5962D9563201QEA	F8859	26CT31D09Q
5962D9563201VEA	F8859	26CT31D09V
5962D9563201QEC	F8859	26CT31D08Q
5962D9563201VEC	F8859	26CT31D08V

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9563201QEC	34371	HS1-26CT31RH-8
5962F9563201VEC	34371	HS1-26CT31RH-Q
5962F9563201QXC	34371	HS9-26CT31RH-8
5962F9563201VXC	34371	HS9-26CT31RH-Q
5962R9563201TEC	34371	HS1-26CT31RH-T
5962R9563201TXC	34371	HS9-26CT31RH-T
5962F9563201V9A	34371	HS0-26CT31RH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation P.O. Box 883 Melbourne, FL 32902-0883
F8859	STMicroelectronics 3, Rue de Suisse BP90294 F-35202 RENNES cedex 2 - France