National Semiconductor

74F112
Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 'F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

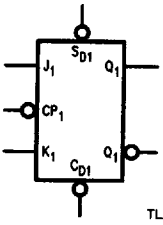
- Guaranteed 4000V minimum ESD protection

Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F112PC	N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
74F112SC (Note 1)	M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F112SJ (Note 1)	M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols



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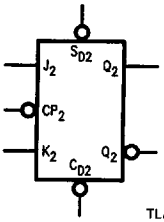

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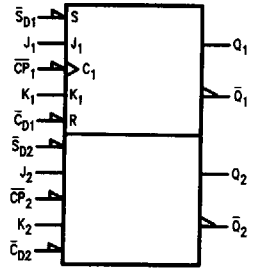
IEEE/IEC



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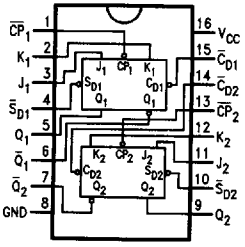
Connection Diagram

Pin Assignment for SOIC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 μA/−2.4 mA
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/5.0	20 μA/−3.0 mA
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA/−3.0 mA
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	−1 mA/20 mA

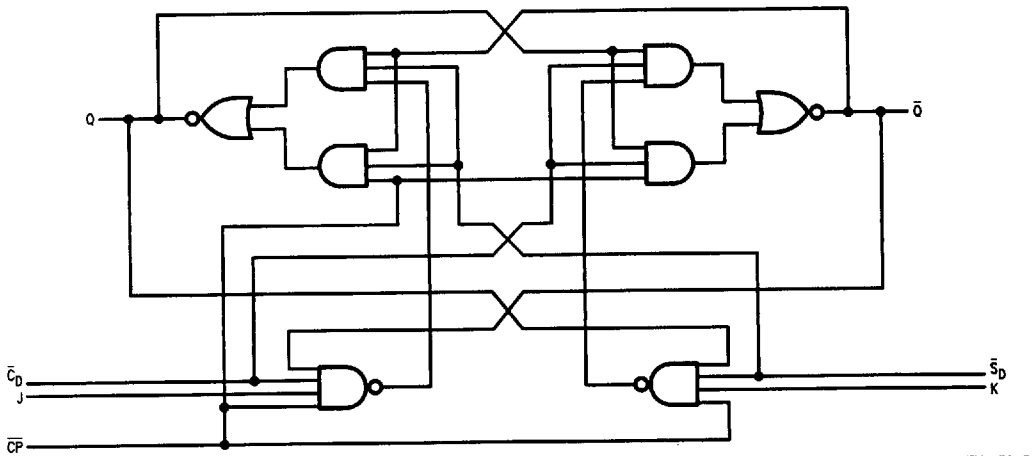
Truth Table

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	h	h	$\overline{Q}_0$	Q_0
H	H	⌐	l	h	L	H
H	H	⌐	h	l	H	L
H	H	⌐	l	l	Q_0	$\overline{Q}_0$

H(h) = HIGH Voltage Level
L(l) = LOW Voltage Level
X = Immaterial
⌐ = HIGH-to-LOW Clock Transition
$Q_0(\overline{Q}_0)$ = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram (One Half Shown)



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F Min	74F Typ	74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All other pins grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All other pins grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (J_n, K_n)
					−2.4			V_{IN} = 0.5V ($\overline{CP}_n$)
					−3.0			V_{IN} = 0.5V ($\overline{C}_{Dn}$, $\overline{S}_{Dn}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			12	19	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			12	19	mA	Max	V_O = LOW

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	85	105		80		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$, $\overline{S}_{Dn}$ to $\overline{Q}_n$, $\overline{Q}_n$	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		74F $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0		5.0 3.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0		0 0			
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	4.5 4.5		5.0 5.0		ns	2-4
$t_w(L)$	Pulse Width, LOW $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	4.5		5.0		ns	2-4
t_{rec}	Recovery Time $\overline{S}_{Dn}$, $\overline{C}_{Dn}$ to $\overline{CP}$	4.0		5.0		ns	2-6