

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

T-66-21-51

**Dual 4-Input Data Selector/
Multiplexer
High-Performance Silicon-Gate CMOS**

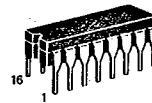
The MC54/74HC153 is identical in pinout to the LS153. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The Address Inputs select one of four Data Inputs from each multiplexer. Each multiplexer has an active-low Strobe control and a noninverting output.

The HC153 is similar in function to the HC253, which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates

MC54/74HC153



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-06**



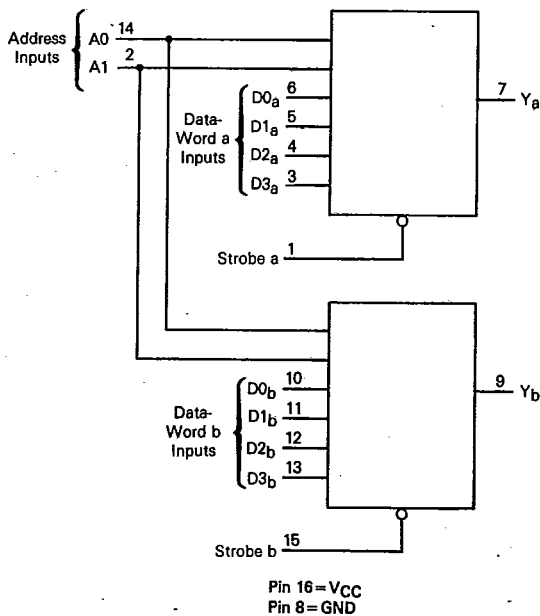
**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

MC74HCXXXN Plastic
MC54HCXXXJ Ceramic
MC74HCXXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Strobe a	1	16	VCC
A1	2	15	Strobe b
D3a	3	14	A0
D2a	4	13	D3b
D1a	5	12	D2b
D0a	6	11	D1b
Ya	7	10	D0b
GND	8	9	Yb

FUNCTION TABLE

Inputs			Output
A1	A0	Strobe	Y
X	X	H	L
L	L	L	D0
L	H	L	D1
H	L	L	D2
H	H	L	D3

D0, D1, D2, and D3= the level of the respective Data Input

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package‡	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-65	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} =2.0 V V _{CC} =4.5 V V _{CC} =6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} =V _{CC} or GND	2.0	0.26	0.33	0.40	μA
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} =V _{CC} or GND I _{out} =0 μA	6.0	±0.1	±1.0	±1.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Output Y (Figures 1 and 4)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Strobe to Output Y (Figures 3 and 4)	2.0	95	120	145	ns
		4.5	19	24	29	
		6.0	16	20	25	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Multiplexer) Used to determine the no-load dynamic power consumption: P _D = CPD V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} = 5.0 V	pF
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SWITCHING WAVEFORMS

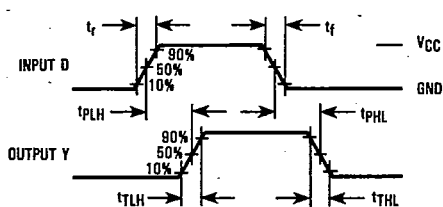


Figure 1

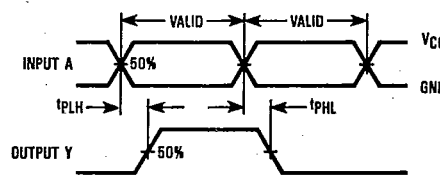


Figure 2

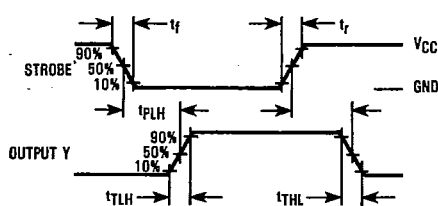
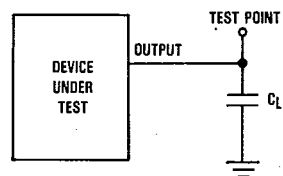


Figure 3



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

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PIN DESCRIPTIONS

DATA INPUTS

D0_a-D3_a, D0_b-D3_b (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Data Inputs. With the outputs enabled, the addressed Data Inputs appear at the Y outputs.

STROBE (PINS 1, 15) — Active-low Strobe. A low level applied to these pins enables the corresponding outputs.

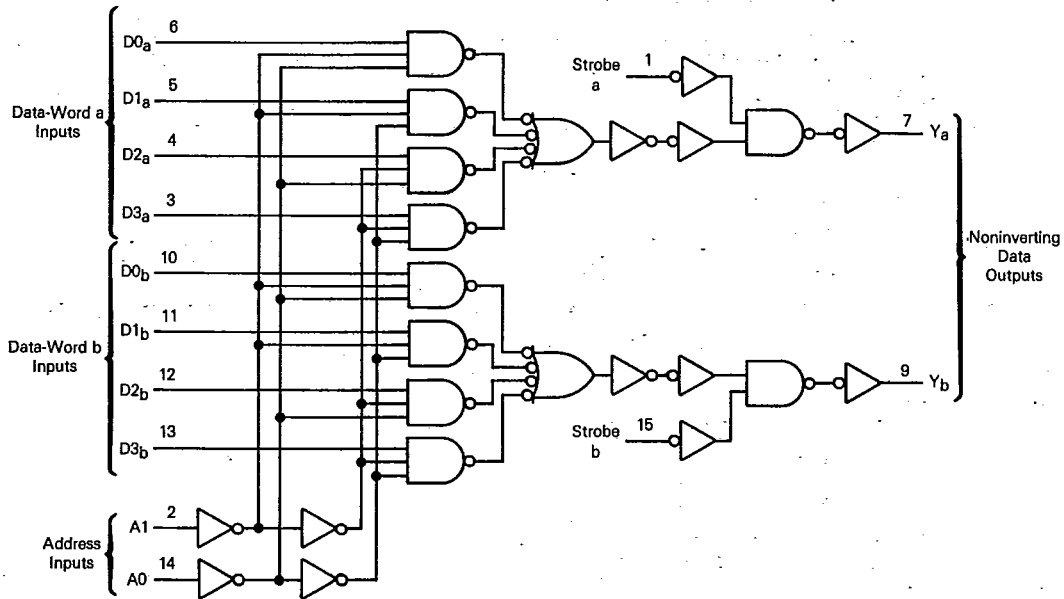
OUTPUTS

Y_a, Y_b (PINS 7, 9) — Noninverting data outputs.

CONTROL INPUTS

A0, A1 (PINS 2, 14) — Address Inputs. These inputs address the pair of Data Inputs which appear at the corresponding outputs.

EXPANDED LOGIC DIAGRAM



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