

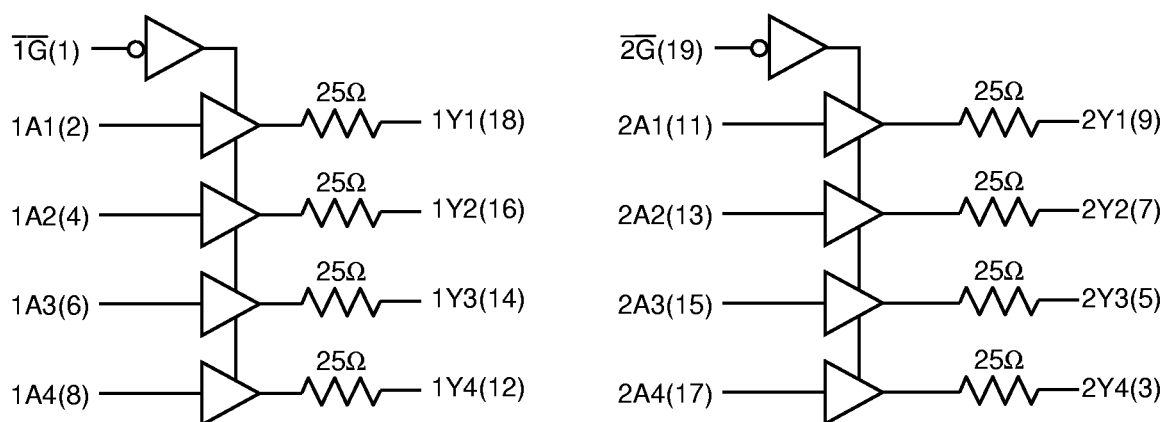
FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- 25Ω series resistor for low switching noise
- 10μA I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V–3.6V V_{CC} supply operation
- ±12mA balanced output drive
- Power down high impedance inputs and outputs
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:
 –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
 Human body model > 2000V
 Machine model > 200V
- Packages available:
 20-pin QSOP
 20-pin SOIC

DESCRIPTION

The LVC2244A is an 8-bit buffer/line driver with three-state outputs that are ideal for driving high capacitance loads such as memory address and data buses. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end, advanced workstation applications. 5V tolerant inputs and outputs allow these LVC products to be used in mixed 5V and 3.3V applications. The LVC2244A with integrated output resistor is ideally suited for low noise environments where reduced output overshoot and undershoot are critical requirements. To accommodate hot-plug or live insertion applications, these products are designed not to load an active bus when V_{CC} is removed. However, during power up or power down sequence, OE should be tied to V_{CC} to ensure high-impedance state on the outputs.

Figure 1. Functional Block Diagram



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Figure 2. Pin Configuration
(All Pins Top View)

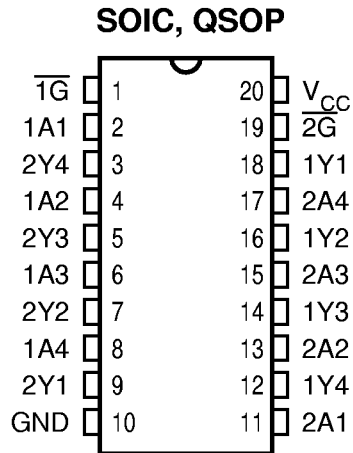


Table 1. Pin Description

| Name | I/O | Description |
|-----------------|-----|---------------------------|
| xA4-xA0 | I | Data Inputs |
| xY4-xY0 | O | Three-State Data Outputs |
| $\overline{1G}$ | I | Three-State Output Enable |
| $\overline{2G}$ | I | Three-State Output Enable |

Table 2. Function Table

| $\overline{1G}/\overline{2G}$ | Input A | Output Y |
|-------------------------------|---------|----------|
| H | X | Z |
| L | L | H |
| L | H | L |

Table 3. Absolute Maximum Ratings

| | |
|---|--------------------------|
| Supply Voltage to Ground | -0.5V to 7.0V |
| DC Output Voltage V_{OUT} | |
| Outputs HIGH-Z | -0.5V to 7.0V |
| Outputs Active | -0.5V to $V_{CC} + 0.5V$ |
| DC Input Voltage V_{IN} | -0.5V to 7.0V |
| DC Input Diode Current with $V_{IN} < 0$ | -50mA |
| DC Output Diode Current | |
| $V_O < 0$ | -50mA |
| $V_O > V_{CC}$ | 50mA |
| DC Output Source/Sink Current (I_{OH}/I_{OL}) | $\pm 50mA$ |
| DC Supply Current per Supply Pin | $\pm 100mA$ |
| DC Ground Current per Ground Pin | $\pm 100mA$ |
| T_{STG} Storage Temperature | -65°C to 150°C |

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

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Table 4. Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit | |
|------------------|-------------------------------------|-------------------------------|-----------------|------|----|
| V _{CC} | Supply Voltage, Operating | 2.0 | 3.6 | V | |
| | Supply Voltage, Data Retention Only | 1.5 | 3.6 | | |
| V _{IH} | Input HIGH Voltage | V _{OL} = 2.7 to 3.6V | 2.0 | — | V |
| V _{IL} | Input LOW Voltage | V _{CC} = 2.7 to 3.6V | — | 0.8 | V |
| V _{IN} | Input Voltage | 0 | 5.5 | V | |
| V _{OUT} | Output Voltage in Active State | 0 | V _{CC} | V | |
| | Output Voltage in "OFF" State | 0 | 5.5 | | |
| I _{OH} | Output Current HIGH | V _{CC} = 3.0–3.6V | — | –12 | mA |
| | | V _{CC} = 2.7V | — | –8 | |
| I _{OL} | Output Current LOW | V _{CC} = 3.0–3.6V | — | 12 | mA |
| | | V _{CC} = 2.7V | — | 8 | |
| Δt/Δv | Input Transition Slew Rate | — | 10 | ns/V | |
| T _A | Operating Free Air Temperature | –40 | 85 | °C | |

Table 5. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, T_A = –40°C to 85°C

| Symbol | Parameter | Test Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|------------------|---|---|-----------------------|--------------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = 2.7V, I _{OH} = –100μA | V _{CC} – 0.2 | — | — | V |
| | | V _{CC} = 2.7V, I _{OH} = –4mA | 2.2 | — | — | |
| | | V _{CC} = 3.0V, I _{OH} = –6mA | 2.4 | — | — | |
| | | V _{CC} = 2.7V, I _{OH} = –8mA | 2.0 | — | — | |
| | | V _{CC} = 3.0V, I _{OH} = –12mA | 2.2 | — | — | |
| V _{OL} | Output LOW Voltage | V _{CC} = 2.7V, I _{OL} = 100μA | — | — | 0.2 | V |
| | | V _{CC} = 2.7V, I _{OL} = 4mA | — | — | 0.4 | |
| | | V _{CC} = 3.0V, I _{OL} = 6mA | — | — | 0.55 | |
| | | V _{CC} = 2.7V, I _{OL} = 8mA | — | — | 0.6 | |
| | | V _{CC} = 3.0V, I _{OL} = 12mA | — | — | 0.8 | |
| V _{IK} | Input Clamp Voltage | V _{CC} = 2.7V, I _{IN} = –18mA | — | –0.7 | –1.2 | V |
| I _I | Input Leakage Current | V _I = 0V, V _I = 5.5V, V _{CC} = 3.6V | — | — | ±1.0 | μA |
| I _{OZ} | High-Z I/O Leakage | V _O = 0V, V _O = 5.5V, V _I = V _{IH} or V _{IL} , V _{CC} = 3.6V | — | — | ±1.0 | μA |
| I _{OFF} | Power Off Leakage | V _{CC} = 0V, V _I or V _O = 5.5V | — | — | 10 | μA |
| I _{CC} | Quiescent Power Supply Current | V _{CC} = 3.6V, V _{IN} = V _{CC} or GND | — | 0.1 | 10 | μA |
| ΔI _{CC} | Quiescent Power Supply Current per Control Inputs at TTL HIGH | V _{CC} = 3.6V, V _{IN} = V _{CC} – 0.6V ⁽²⁾ | — | 2.0 | 3.0 | μA |

Notes:

1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
2. Per TTL driven input. All other inputs at V_{CC} or GND.

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Table 6. Dynamic Switching Characteristics

| Symbol | Parameter | Test Conditions | Typ ⁽¹⁾ | Unit | |
|------------------|---|---|--------------------|------|----|
| V _{OLP} | Quiet Output Dynamic Peak V _{OL} | C _L = 50pF, V _{CC} = 3.3V V _{IH} = 3.3V, V _{IL} = 0V | 0.8 | V | |
| V _{OLV} | Quiet Output Dynamic Valley V _{OL} | C _L = 50pF, V _{CC} = 3.3V V _{IH} = 3.3V, V _{IL} = 0V | 0.8 | V | |
| C _{PD} | Power Dissipation | C _L = 50pF, f = 10MHz, V _{CC} = 3.3 ±0.3V | Output Enable | 20 | pF |
| | | | Output Disable | 4 | |

Note:

1. Typical values are at V_{CC} = 3.3V, 25°C ambient.

Table 7. Capacitance⁽¹⁾

| Symbol | Pins | Conditions | Typ | Unit |
|------------------|-------------------|---|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz | 7.0 | pF |
| C _{I/O} | I/O Capacitance | V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz | 8.0 | pF |

Note:

1. Capacitance is characterized but not production tested.

Table 8. Switching Characteristics Over Operating Range

Industrial Temperature Range, T_A = -40°C to 85°C.

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

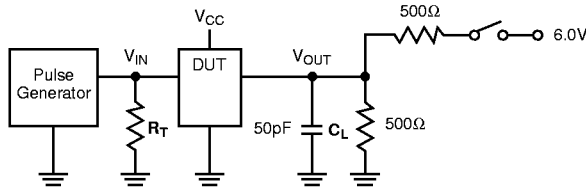
| Symbol | Description ⁽¹⁾ | V _{CC} = 3.3 ±0.3V | | V _{CC} = 2.7V ⁽²⁾ | | Unit |
|--------------------|---|-----------------------------|-----|---------------------------------------|-----|------|
| | | Min | Max | Min | Max | |
| t _{PD} | Propagation Delay xAx to xYx | 1.5 | 5.5 | 1.5 | 6.4 | ns |
| t _{EN} | Output Enable Time x $\overline{\text{OE}}$ to xYx | 1.5 | 7.1 | 1.5 | 8.1 | ns |
| t _{DIS} | Output Disable Time ⁽²⁾ x $\overline{\text{OE}}$ to xYx | 1.5 | 6.8 | 1.5 | 7.3 | ns |
| t _{SK(O)} | Output Skew ⁽³⁾ | — | 0.5 | — | — | ns |

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



| SWITCH POSITION | |
|------------------|--------|
| Test | Switch |
| Open Drain | |
| Disable LOW | 6V |
| Enable LOW | |
| Disable HIGH | GND |
| Enable HIGH | |
| All Other Inputs | Open |

DEFINITIONS:
 C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing

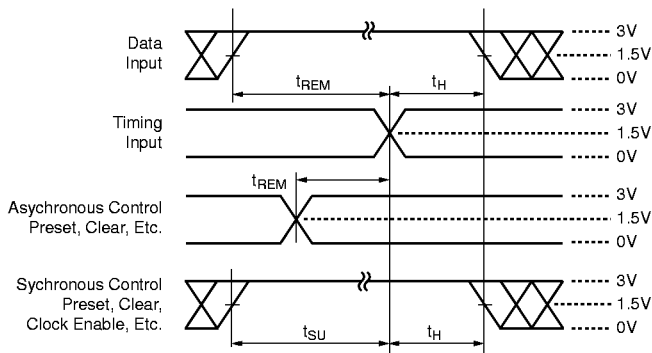


Figure 6. Pulse Width

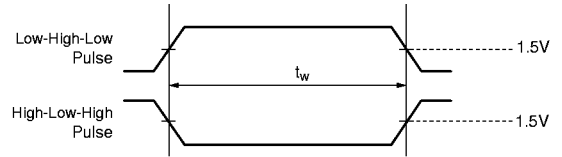
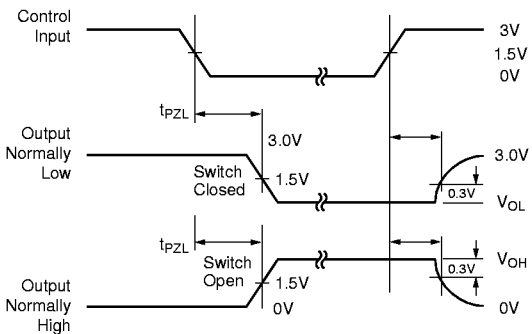


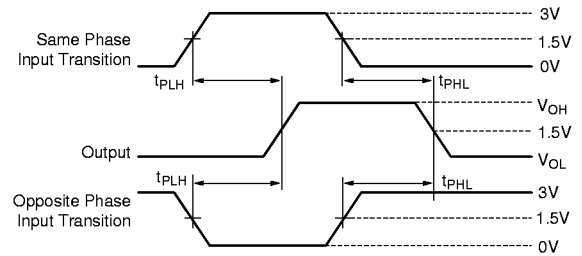
Figure 5. Enable and Disable Timing



Notes:

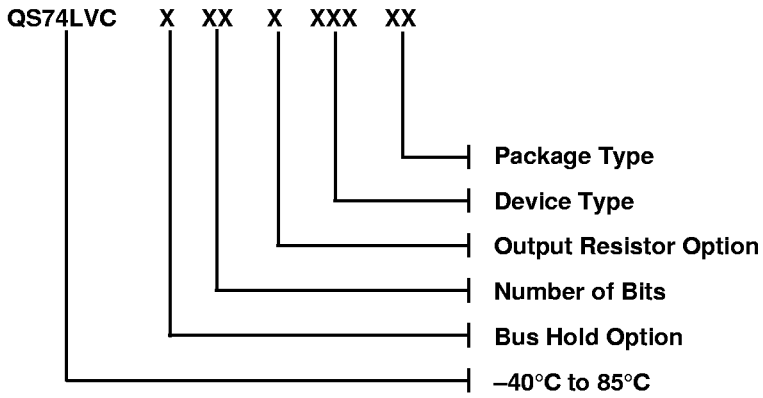
1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz;
 $Z_{OUT} \leq 50\Omega$; $t_F, t_R \leq 2.5ns$.

Figure 7. Propagation Delay



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ORDERING INFORMATION



Bus Hold Option:
Blank – No Bus Hold

Number of Bits:
Blank – 8-Bit

Output Resistor Option:
2 – Output Resistor

Device Type:
244

Package Type:
Q – QSOP, 150 mil
SO – SOIC, 300 mil