National Semiconductor

74VHC32
Quad 2-Input OR Gate

General Description

The VHC32 is an advanced high speed CMOS 2-Input OR Gate fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- All inputs are equipped with a Power Down Protection Function
- Balanced Propagation Delays: $t_{PLH} \cong t_{PHL}$
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with 74HC32

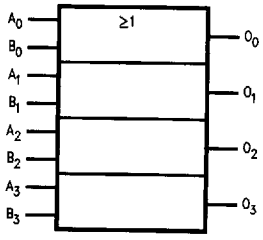
Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC32M	M14A	14-Lead Molded JEDEC SOIC
74VHC32SJ	M14D	14-Lead Molded EIAJ SOIC
74VHC32MSC	MSC14	14-Lead Molded EIAJ Type 1 SSOP
74VHC32MTC	MTC14	14-Lead Molded JEDEC Type 1 TSSOP
74VHC32N	N14A	14-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
EIAJ Type I SSOP available Tape and Reel only, order MSCX.

Logic Symbol

IEEE/IEC



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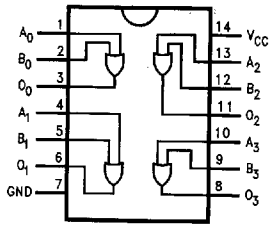
Connection Diagram

Pin Assignment for DIP, SSOP, TSSOP and SOIC



TL/F/11518–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Truth Table

A	B	O
H	H	H
L	H	H
H	L	H
L	L	L

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C			74VHC T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Typ	74VHC $T_A = 25°C$ Limit	Units	Conditions	Fig. No.
**V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.3	0.8	V	C_L = 50 pF	2-11, 12
**V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.3	−0.8	V	C_L = 50 pF	2-11, 12
**V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF	2-11, 12
**V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF	2-11, 12

**Parameter guaranteed by design.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Min	Typ	Max	74VHC $T_A = -40°C$ to $+85°C$ Min	Max	Units	Test Condition	Fig. No.
t_{PHL}, t_{PLH}	Propagation Delay	3.3 ±0.3		5.5	7.9	1.0	9.5	ns	C_L = 15 pF	2-5
				8.0	11.4	1.0	13.0		C_L = 50 pF	
		5.0 ±0.5		3.8	5.5	1.0	6.5	ns	C_L = 15 pF	2-5
				5.3	7.5	1.0	8.5		C_L = 50 pF	
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{PD}	Power Dissipation Capacitance			14				pF	(Note 1)	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per gate).