## INTEGRATED CIRCUITS

# DATA SHEET

**74LVC02**Quad 2-input NOR gate

Product specification

1997 Feb 03

IC24 Data Handbook





## Quad 2-input NOR gate

74LVC02

#### **FEATURES**

- Wide supply voltage: 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

#### DESCRIPTION

The 74LVC02 is a high performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC02 provides the 2-input NOR function.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}C$ ;  $t_r = t_f \le 2.5 \text{ ns}$ 

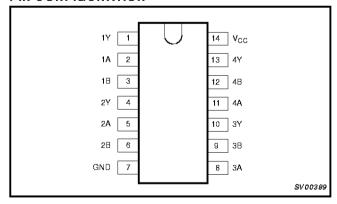
SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation delay nA, nB to nY	$\begin{array}{l} C_L = 50 \text{ pF}; \\ V_{CC} = 3.3 \text{ V} \end{array} \label{eq:classical_constraints}$	3.3	ns
C <sub>I</sub>	Input capacitance		5.0	pF
C <sub>PD</sub>	Power dissipation capacitance per gate	Notes 1 and 2	60	pF

- 1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_{D}$  in  $\mu W$ )
  - $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:
- f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacity in pF;
   f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;
   ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.
   The condition is V<sub>I</sub> = GND to V<sub>CC</sub>.

#### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	−40°C to +85°C	74LVC02 D	74LVC02 D	SOT108-1
14-Pin Plastic SSOP Type II	−40°C to +85°C	74LVC02 DB	74LVC02 DB	SOT337-1
14-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVC02 PW	74LVC02PW DH	SOT402-1

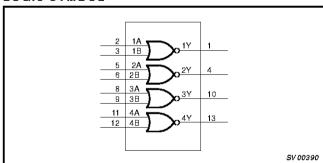
#### **PIN CONFIGURATION**



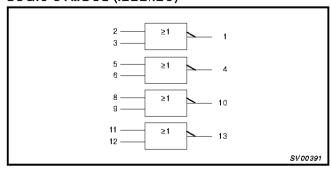
#### **PIN DESCRIPTION**

PIN Number	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y – 4Y	Data outputs
2, 5, 8, 11	1A – 4A	Data inputs
3, 6, 9, 12	<b>1</b> B – 4B	Data inputs
7	GND	Ground (0 V)
14	$V_{\rm CC}$	Positive supply voltage

#### LOGIC SYMBOL



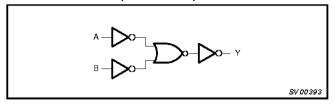
#### LOGIC SYMBOL (IEEE/IEC)



## Quad 2-input NOR gate

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#### LOGIC DIAGRAM (ONE GATE)



#### **FUNCTION TABLE**

INP	OUTPUTS	
n A	nB	nΥ
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

#### NOTES:

H = HIGH voltage level L = LOW voltage level

#### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIM	TINU		
STINBUL	PARAMETER	CONDITIONS	MIN	MAX	] """	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	٧	
$V_{\rm CC}$	DC supply voltage (for low-voltage applications)		1.2	3.6	٧	
V <sub>I</sub>	DC input voltage range		0	5.5	٧	
V <sub>I/O</sub>	DC input voltage range for I/Os		0	V <sub>CC</sub>	٧	
V <sub>O</sub>	DC output voltage range		0	$V_{\rm CC}$	٧	
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C	
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	$V_{CC} = 1.2 \text{ to } 2.7V$ $V_{CC} = 2.7 \text{ to } 3.6V$	0 0	20 10	ns/V	

#### ABSOLUTE MAXIMUM RATINGS1

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT	
V <sub>CC</sub>	DC supply voltage		-0.5 to +6.5		
l <sup>IK</sup>	DC input diode current	V <sub>I</sub> < 0	_50 m₁		
V <sub>I</sub>	DC input voltage	Note 2	-0.5 to +5.5 \		
V <sub>I/O</sub>	DC input voltage range for I/Os		-0.5 to V <sub>CC</sub> +0.5	V	
lok	DC output diode current	$V_{\rm O} > V_{\rm CC}$ or $V_{\rm O} < 0$	±50	mA	
V <sub>OUT</sub>	DC output voltage	Note 2	-0.5 to V <sub>CC</sub> +0.5		
l <sub>OUT</sub>	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA	
I <sub>GND</sub> , I <sub>CC</sub>	DC V <sub>CC</sub> or GND current		±100	mA	
T <sub>stg</sub>	Storage temperature range		-60 to + <b>1</b> 50	°C	
P <sub>TOT</sub>	Power dissipation per package  – plastic mini-pack (SO)  – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW	

#### NOTES:

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2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the
device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to
absolute-maximum-rated conditions for extended periods may affect device reliability.

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#### DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

			L	UNIT			
SYMBOL	PARAMETER	TEST CONDITIONS	Temp = -				
			MIN	TYP1	MAX	1	
M	HICH I I I t It	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.7 to 3.6V	2.0			1 °	
	LOW loved lower treated	V <sub>CC</sub> = 1.2V			GND	V	
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.7 to 3.6V			0.8	1 °	
		$V_{CC} = 2.7V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -12mA$	$V_{\rm CC} - 0.5$				
V <sub>OH</sub>	HIGH level output voltage	$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -100\mu A$	$V_{CC} - 0.2$	$V_{CC}$		] <sub>v</sub>	
		$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = -12\text{mA}$	V <sub>CC</sub> -0.6				
		$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -24mA$	V <sub>CC</sub> - 1.0			1	
		$V_{CC} = 2.7V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 12mA$			0.40		
$V_{OL}$	LOW level output voltage	$V_{CC}=3.0V;\ V_I=V_{IH}\ or\ V_{IL};\ I_O=100\mu A$		GND	0.20		
		$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 24mA$			0.55		
lį	Input leakage current	$V_{CC} = 3.6V$ ; $V_I = 5.5V$ or GND Not for I/O pins		±0.1	±5	μА	
I <sub>IHZ</sub> /I <sub>ILZ</sub>	Input current for common I/O pins	$V_{CC} = 3.6V$ ; $V_I = V_{CC}$ or GND		±0.1	<b>±1</b> 5	μА	
l <sub>OZ</sub>	3-State output OFF-state current	$V_{CC} = 3.6V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND		0.1	±10	μА	
I <sub>CC</sub>	Quiescent supply current	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or GND}; I_O = 0$		0.1	20	μА	
Δl <sub>CC</sub>	Additional quiescent supply current per input pin	$V_{CC} = 2.7V$ to 3.6V; $V_I = V_{CC} - 0.6V$ ; $I_O = 0$		5	500	μА	

#### NOTE

#### **AC CHARACTERISTICS**

GND = 0 V;  $t_r$  =  $t_f$   $\leq$  2.5 ns;  $C_L$  = 50 pF;  $R_L$  = 500 $\Omega$ ;  $T_{amb}$  = -40°C to +85°C

			LIMITS							
SYMBO L	PARAMETER	WAVEFORM	V <sub>CC</sub> = 3.3V ±0.3V		V <sub>CC</sub> = 2.7V			V <sub>CC</sub> = 1.2V	UNIT	
			MIN	TYP1	MAX	MIN	TYP1	MAX	TYP	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nA, nB to nY	Figures 1, 2	1.5	3.5	6.0	1.5	4.0	6.5	20	ทธ

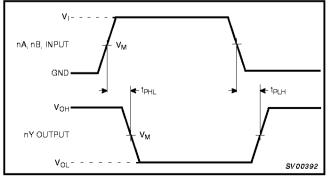
#### NOTE:

1. These typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^{\circ}C$ .

### **AC WAVEFORMS**

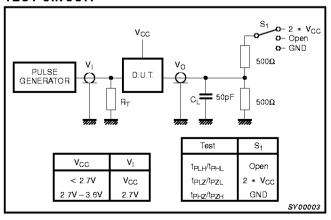
 $V_M = 1.5 \text{ V at } V_{CC} \ge 2.7 \text{ V}$  $V_M = 0.5 \bullet V_{CC} \text{ at } V_{CC} < 2.7 \text{ V}$ 

 $\ensuremath{V_{OL}}$  and  $\ensuremath{V_{OH}}$  are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB) to output (nY) propagation delays.

#### **TEST CIRCUIT**



Waveform 2. Load circuitry for switching times.

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<sup>1.</sup> All typical values are at  $V_{CC}=3.3V$  and  $T_{amb}=25^{\circ}C$ .

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

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Quad 2-input NOR gate

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

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Quad 2-input NOR gate

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

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