REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Paragraph 1.3 absolute maximum, correct input voltage range. Editorial changes throughout.	90-08-14	W. K. Heckman
B	Add vendor cage 0DKS7. Add device type 03. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout – jak.	01-03-05	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13		

PMIC N/A

PREPARED BY
Greg A. Pitz

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raymond Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-03-08

MICROCIRCUIT, DIGITAL, BIPOLAR HIGH PERFORMANCE 10-BIT BUFFER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
B	A	**67268**	**5962-88605**

SHEET 1 OF 13

DSCC FORM 2233
APR 97

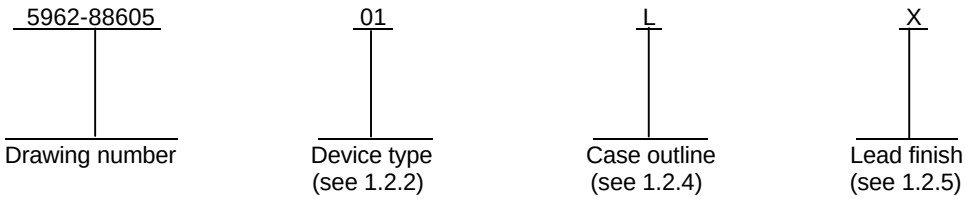
5962-E051-01

1. SCOPE

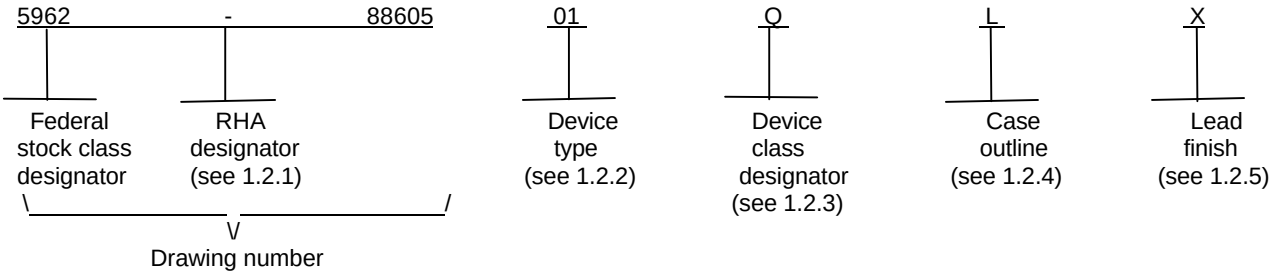
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For devices 01 - 02:



For device 03



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29827A	High performance 10-bit inverting buffer, three-state
02	29828A	High performance 10-bit inverting buffer, three-state
03	29827A	High performance 10-bit inverting buffer, three-state

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, for device types 01 and 02 device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-1.5 V dc to 6.0 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to 5.5 V dc
DC output current into output	+100 mA
DC output current out of output	-50 mA
DC input current into input	-30 mA to +5.0 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D) 2/	1.82 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case temperature operating range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 2 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = -15 mA	All	1, 2, 3	2.4		V
			I_{OH} = -24 mA			2.0		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V, I_{OL} = 32 mA		All	1, 2, 3		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA		All	1, 2, 3		-1.2	V
Input hysteresis	V_{HYST}			01, 02	1, 2, 3	200		mV
				03	1, 2, 3	150		
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		All	1, 2, 3		-0.5	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} 2.7 V		All	1, 2, 3		50	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} 5.5 V		All	1, 2, 3		100	
Offstate output current	I_{OZH}	V_{CC} = 5.5 V, V_{OUT} 2.7 V		All	1, 2, 3		50	µA
	I_{OZL}	V_{CC} = 5.5 V, V_{OUT} = 0.4 V					-50	
Short circuit output current	I_{OS} 1/	V_{CC} = 5.5 V, V_{OUT} = 0.0 V		All	1, 2, 3	-75	-250	mA
Bus leakage current	I_{OFF}	V_{CC} = 0.0 V, V_{OUT} = 2.9 V		All	1, 2, 3		100	µA
Supply current	I_{CC}	V_{CC} = 5.5 V Outputs open V_{IL} = 0.8 V V_{IH} = 2.0 V	Outputs logic low	All			80.0	mA
			Outputs logic high	All			55.0	
			Outputs logic three-state	All			70.0	
Functional tests		V_{CC} = 5.5 V See 4.4.1c		All	7, 8	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, from Di to Yi	t_{PLH}	V_{CC} = 5.0 V C_L = 50 pF ±10% R_1 = 500Ω, R_2 = 500Ω See figure 4	01, 03	9, 10, 11		9.0	ns
			02			8.0	
	t_{PHL}		01, 03	9, 10, 11		9.0	
			02			10.0	
Propagation delay time, output enable, from OEi to Yi or Yi	t_{PZH}	V_{CC} = 5.0 V C_L = 50 pF ±10% R_1 = 500Ω, R_2 = 500Ω See figure 4	01, 02	9, 10, 11		12.0	ns
			03			14.0	
	t_{PZL}		01, 02	9, 10, 11		13.0	
			03			15.0	
Propagation delay time, output disable, from OEi to Yi or Yi	t_{PHZ}	V_{CC} = 5.0 V C_L = 50 pF ±10% R_1 = 500Ω, R_2 = 500Ω See figure 4	All	9, 10, 11		10.0	ns
	t_{PLZ}		01, 02	9, 10, 11		10.0	
			03			12.0	

1/ Not more than one output should be shorted at a time and the duration of the short circuit condition should not exceed 100 milliseconds.

Device types	01, 03	02	01, 03	02
Case outlines	K and L		3	
Terminal number	Terminal symbol			
1	$\overline{OE1}$	$\overline{OE1}$	NC	NC
2	D0	D0	$\overline{OE1}$	$\overline{OE1}$
3	D1	D1	D0	D0
4	D2	D2	D1	D1
5	D3	D3	D2	D2
6	D4	D4	D3	D3
7	D5	D5	D4	D4
8	D6	D6	NC	NC
9	D7	D7	D5	D5
10	D8	D8	D6	D6
11	D9	D9	D7	D7
12	GND	GND	D8	D8
13	$\overline{OE2}$	$\overline{OE2}$	D9	D9
14	Y9	Y9	GND	GND
15	Y8	Y8	NC	NC
16	Y7	Y7	$\overline{OE2}$	$\overline{OE2}$
17	Y6	Y6	Y9	Y9
18	Y5	Y5	Y8	Y8
19	Y4	Y4	Y7	Y7
20	Y3	Y3	Y6	Y6
21	Y2	Y2	Y5	Y5
22	Y1	Y1	NC	NC
23	Y0	Y0	Y4	Y4
24	V_{CC}	V_{CC}	Y3	Y3
25	- - -	- - -	Y2	Y2
26	- - -	- - -	Y1	Y1
27	- - -	- - -	Y0	Y0
28	- - -	- - -	V_{CC}	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Device types 01 and 03

Inputs			Ouputs	Function
$\overline{OE1}$	$\overline{OE2}$	Di	Yi	
L	L	H	H	Data output
L	L	L	L	Transparent
X	H	X	Z	High impedance
H	X	X	Z	High impedance

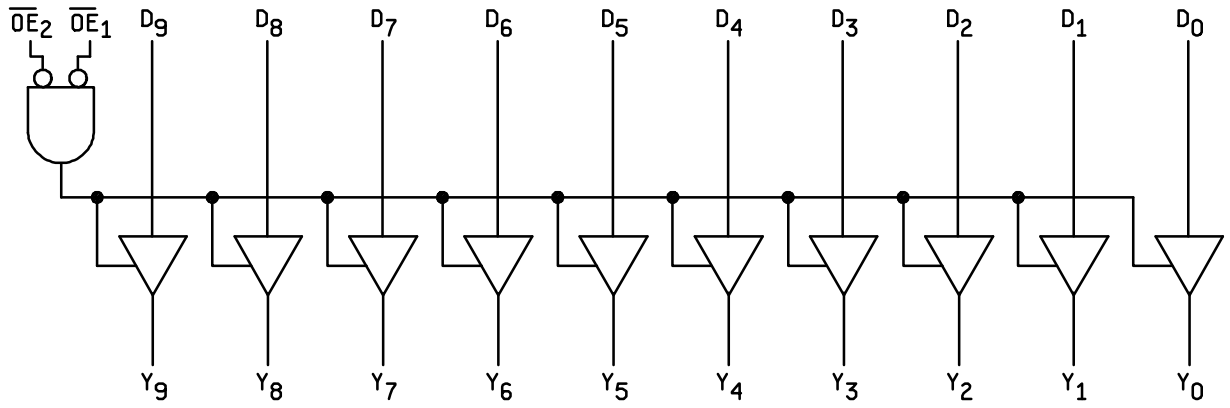
Device type 02

Inputs			Ouputs	Function
$\overline{OE1}$	$\overline{OE2}$	Di	$\overline{Yi}$	
L	L	H	L	Data output
L	L	L	H	Transparent
X	H	X	Z	High impedance
H	X	X	Z	High impedance

H = High voltage level
L = Low level voltage
X = Irrelevant
Z = High impedance

Figure 2. Truth tables.

DEVICE TYPE 01 AND 03



DEVICE TYPE 02

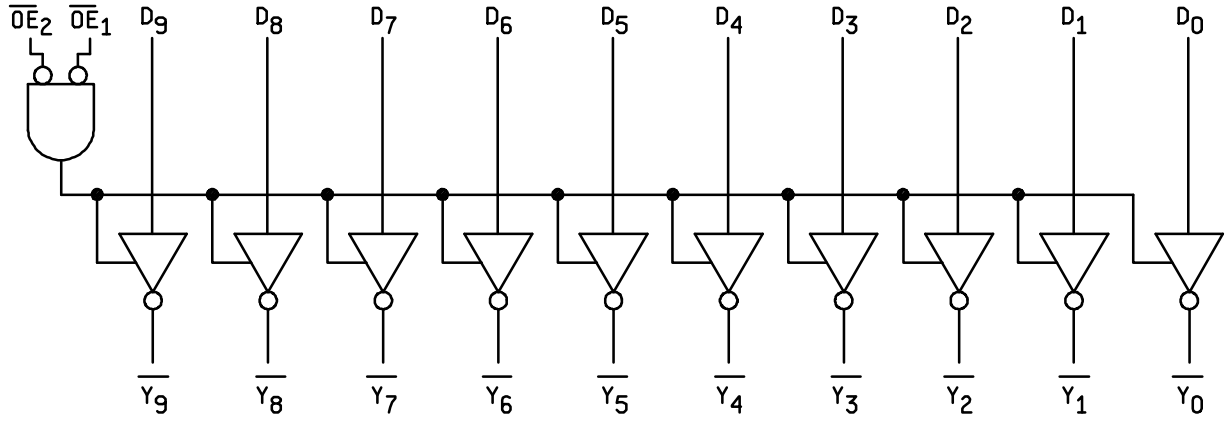
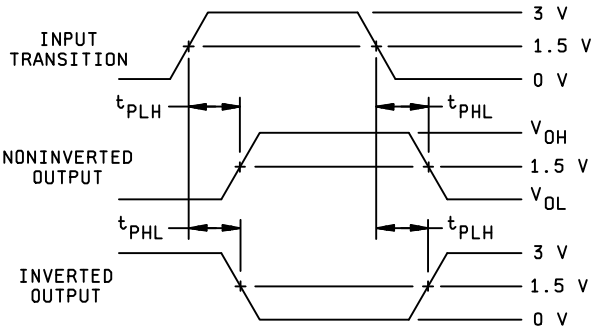
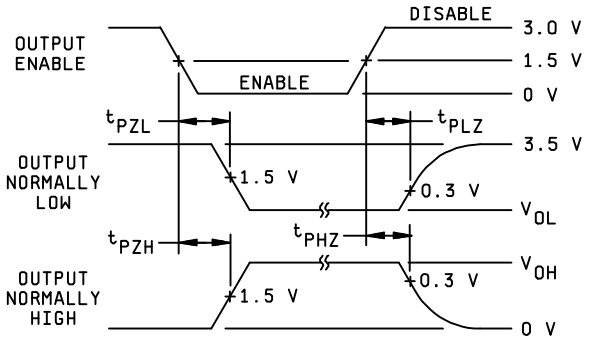


FIGURE 3. Logic diagrams.

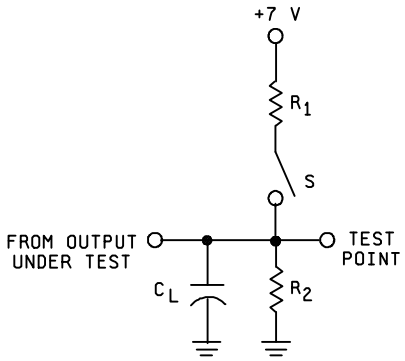
PROPAGATION DELAY



ENABLE AND DISABLE TIMES



SWITCHING TEST CIRCUIT



LOAD CIRCUIT FOR THREE-STATE OUTPUTS

PARAMETER	S POSITION
t_{PLH}	OPEN
t_{PHL}	OPEN
t_{PHZ}	OPEN
t_{PZH}	OPEN
t_{PLZ}	CLOSED
t_{PZL}	CLOSED

SWITCH POSITIONS FOR PARAMETER TESTING

FIGURE 4. Switching waveforms and test circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 are omitted.

c. Subgroups 7 and 8 tests shall verify the truth tables.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	----	----	----

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-03-05

Approved sources of supply for SMD 5962-88605 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML 38535 during the next revision. MIL-HDBK-103 and QML 38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103. and QML 38535

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Generic Part number 2/
5962-8860501LX	3/	AM29827A/BLA	
5962-8860501KX	3/	AM29827A/BKA	
5962-88605013X	3/	AM29827A/B3A	
5962-8860502LX	3/	AM29828A/BLA	
5962-8860502KX	3/	AM29828A/BKA	
5962-88605023X	3/	AM29828A/B3A	
5962-8860503QLA	0DKS7	GEM19303QLA	29827A
5962-8860503QLC	0DKS7	GEM19303QLC	29827A
5962-8860503QKA	0DKS7	GEM19303QKA	29827A
5962-8860503QKC	0DKS7	GEM19303QKC	29827A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0DKS7	David Sarnoff Research Center 201 Washington Road Princeton, NJ 08540-5300