- **Choice of True or Inverting Logic**

- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
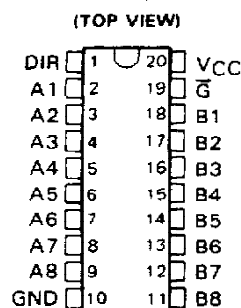
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HC640	Inverting
'HC643	True and Inverting
'HC645	True

SN54HC' . . . J PACKAGE
SN74HC' . . . DW OR N PACKAGE
(TOP VIEW)

DIR	1	20	VCC
A1	2	19	G̅
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

SN54HC' . . . FK PACKAGE
(TOP VIEW)

Top pins: A2, A1, DIR, VCC, G̅ (pins 3, 2, 1, 20, 19)

A3	4	18	B1
A4	5	17	B2
A5	6	16	B3
A6	7	15	B4
A7	8	14	B5

Bottom pins: A8, GND, B8, B7, B6 (pins 9, 10, 11, 12, 13)
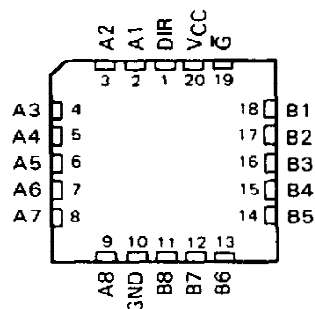
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G̅) can be used to disable the device so the buses are effectively isolated.

The SN54HC640, SN54HC643, and SN54HC645 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC640, SN74HC643, and SN74HC645 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION		
G̅	DIR	'HC640	'HC643	'HC645
L	L	B̅ data to A bus	B data to A bus	B data to A bus
L	H	A̅ data to B bus	A̅ data to B bus	A data to B bus
H	X	Isolation	Isolation	Isolation

TEXAS INSTRUMENTS
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SN54HC640, SN54HC643, SN54HC645
SN74HC640, SN74HC643, SN74HC645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbols†
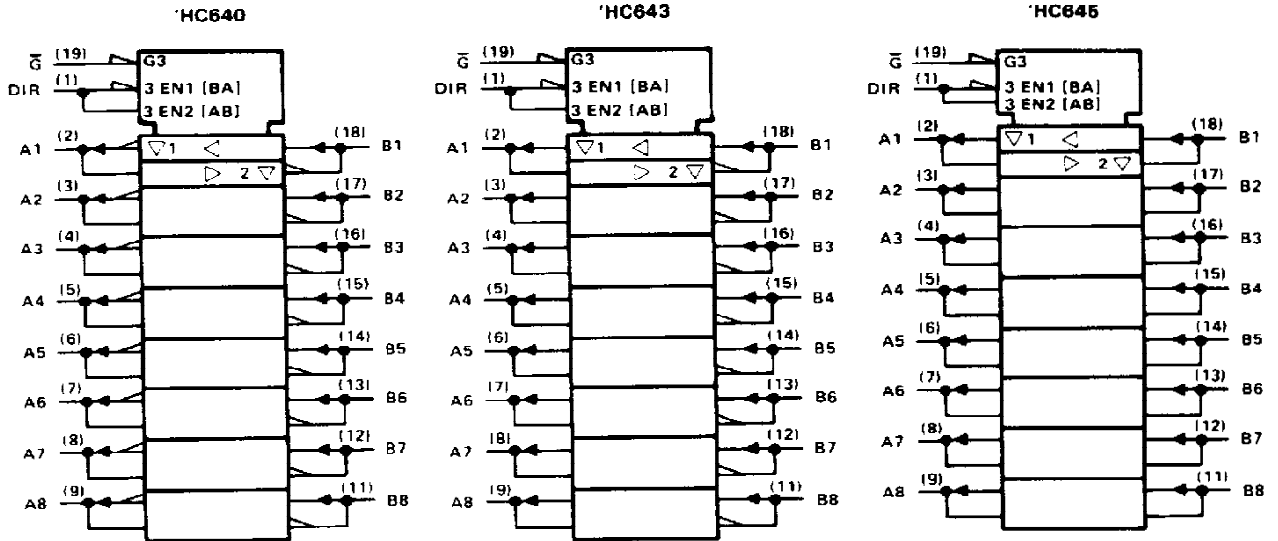
'HC640

'HC643

'HC645

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'HC640

'HC643

'HC645

TO SEVEN OTHER TRANSCEIVERS

TO SEVEN OTHER TRANSCEIVERS

TO SEVEN OTHER TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} .... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
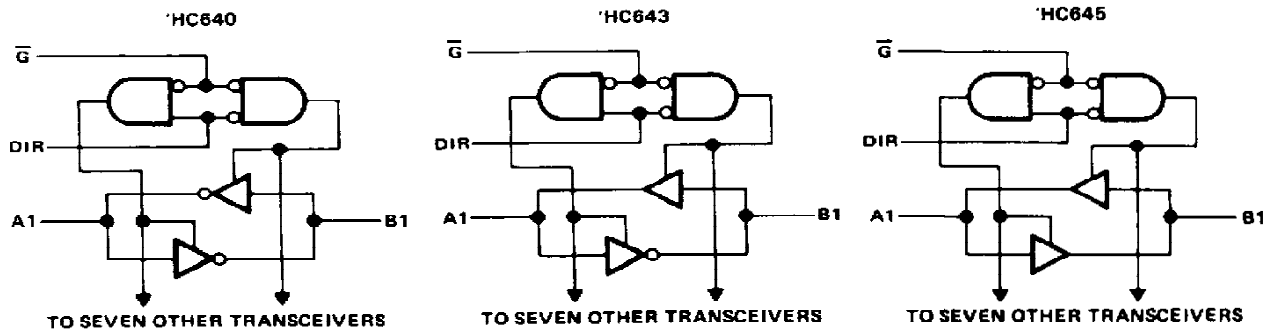Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±35 mA
Continuous current through V_{CC} or GND pins .... ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package .... 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package .... 260°C
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC640 SN54HC643 SN54HC645			SN74HC640 SN74HC643 SN74HC645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
	$V_{CC} = 4.5$ V	3.15			3.15			
	$V_{CC} = 6$ V	4.2			4.2			
V_{IL} Low-level input voltage	$V_{CC} = 2$ V	0		0.3	0		0.3	V
	$V_{CC} = 4.5$ V	0		0.9	0		0.9	
	$V_{CC} = 6$ V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	$V_{CC} = 2$ V	0		1000	0		1000	ns
	$V_{CC} = 4.5$ V	0		500	0		500	
	$V_{CC} = 6$ V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54HC640 SN54HC643 SN54HC645		SN74HC640 SN74HC643 SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -20$ μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -6$ mA	4.5 V	3.98	4.30		3.7		3.84		
		$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -7.8$ mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 20$ μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 6$ mA	4.5 V		0.17	0.26		0.4		0.33	
		$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 7.8$ mA	6 V		0.15	0.26		0.4		0.33	
I_I	DIR or $\overline{G}$	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	$V_O = V_{CC}$ or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	μA
C_i	DIR or $\overline{G}$		2 to 6 V		3	10		10		10	pF

SN54HC640, SN74HC640
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc	T_A = 25°C MIN	TYP	MAX	SN54HC640 MIN	MAX	SN74HC640 MIN	MAX	UNIT
t_{pd}	A or B	B or A	2 V		29	105		160		130	
			4.5 V		10	21		32		26	ns
			6 V		8	18		27		22	
t_{en}	$\overline{G}$	A or B	2 V		109	230		340		290	
			4.5 V		27	46		68		58	ns
			6 V		20	39		58		49	
t_{dis}	$\overline{G}$	A or B	2 V		40	150		225		190	
			4.5 V		18	30		45		38	ns
			6 V		16	26		38		32	
t_t		A or B	2 V		20	60		90		75	
			4.5 V		8	12		18		15	ns
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc	T_A = 25°C MIN	TYP	MAX	SN54HC640 MIN	MAX	SN74HC640 MIN	MAX	UNIT
t_{pd}	A or B	B or A	2 V		44	190		290		235	
			4.5 V		14	38		58		47	ns
			6 V		11	33		49		41	
t_{en}	$\overline{G}$	A or B	2 V		124	315		470		395	
			4.5 V		31	63		94		79	ns
			6 V		23	54		80		68	
t_t		A or B	2 V		45	210		315		265	
			4.5 V		17	42		63		53	ns
			6 V		13	36		53		46	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	TYP	MAX	SN54HC643 MIN	MAX	SN74HC643 MIN	MAX	UNIT
t_{pd}	A or B	B or A	2 V		29	110		165		140	ns
			4.5 V		10	22		33		28	
			6 V		8	19		28		24	
t_{en}	$\overline{G}$	A or B	2 V		109	230		340		290	ns
			4.5 V		27	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{G}$	A or B	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	TYP	MAX	SN54HC643 MIN	MAX	SN74HC643 MIN	MAX	UNIT
t_{pd}	A or B	B or A	2 V		44	195		295		245	ns
			4.5 V		14	39		59		49	
			6 V		11	34		50		43	
t_{en}	$\overline{G}$	A or B	2 V		124	315		470		395	ns
			4.5 V		31	63		94		79	
			6 V		23	54		80		68	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc	T_A = 25°C MIN	TYP	MAX	SN54HC645 MIN	MAX	SN74HC645 MIN	MAX	UNIT
t_{pd}	A or B	B or A	2 V		40	105		160		130	ns
			4.5 V		15	21		32		26	
			6 V		12	18		27		22	
t_{en}	$\overline{G}$	A or B	2 V		125	230		340		290	ns
			4.5 V		23	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{G}$	A or B	2 V		74	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		21	34		51		43	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc	T_A = 25°C MIN	TYP	MAX	SN54HC645 MIN	MAX	SN74HC645 MIN	MAX	UNIT
t_{pd}	A or B	B or A	2 V		54	135		200		170	ns
			4.5 V		18	27		40		34	
			6 V		15	23		34		29	
t_{en}	$\overline{G}$	A or B	2 V		150	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		25	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87809012A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87809012A SNJ54HC 640FK	
5962-8780901RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780901RA SNJ54HC640J	Samples
SN54HC640J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC640J	Samples
SN54HC645J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC645J	Samples
SN74HC640DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC640N	Samples
SN74HC640NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC640N	Samples
SN74HC640NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC645DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC645	Samples
SN74HC645DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC645	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC645DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC645	Samples
SN74HC645N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC645N	Samples
SN74HC645NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC645N	Samples
SNJ54HC640FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87809012A SNJ54HC 640FK	
SNJ54HC640J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780901RA SNJ54HC640J	Samples
SNJ54HC645FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54HC 645FK	Samples
SNJ54HC645J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54HC645J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC640, SN54HC645, SN74HC640, SN74HC645 :

● Catalog: SN74HC640, SN74HC645

● Military: SN54HC640, SN54HC645

NOTE: Qualified Version Definitions:

  ● Catalog - TI's standard catalog product

  ● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC640DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC640NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74HC640PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HC645DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC640DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC640NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC640PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74HC645DWR	SOIC	DW	20	2000	367.0	367.0	45.0

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$ 0.050 (1,27) $\frac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a metal lid.
          D.   Falls within JEDEC MS−004

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N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
   △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
   △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6 ←| |←   →| |← 18x1,27

9,4

→| |← 20x0,55   →| |← 18x1,27

20x1,95 ←|

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around
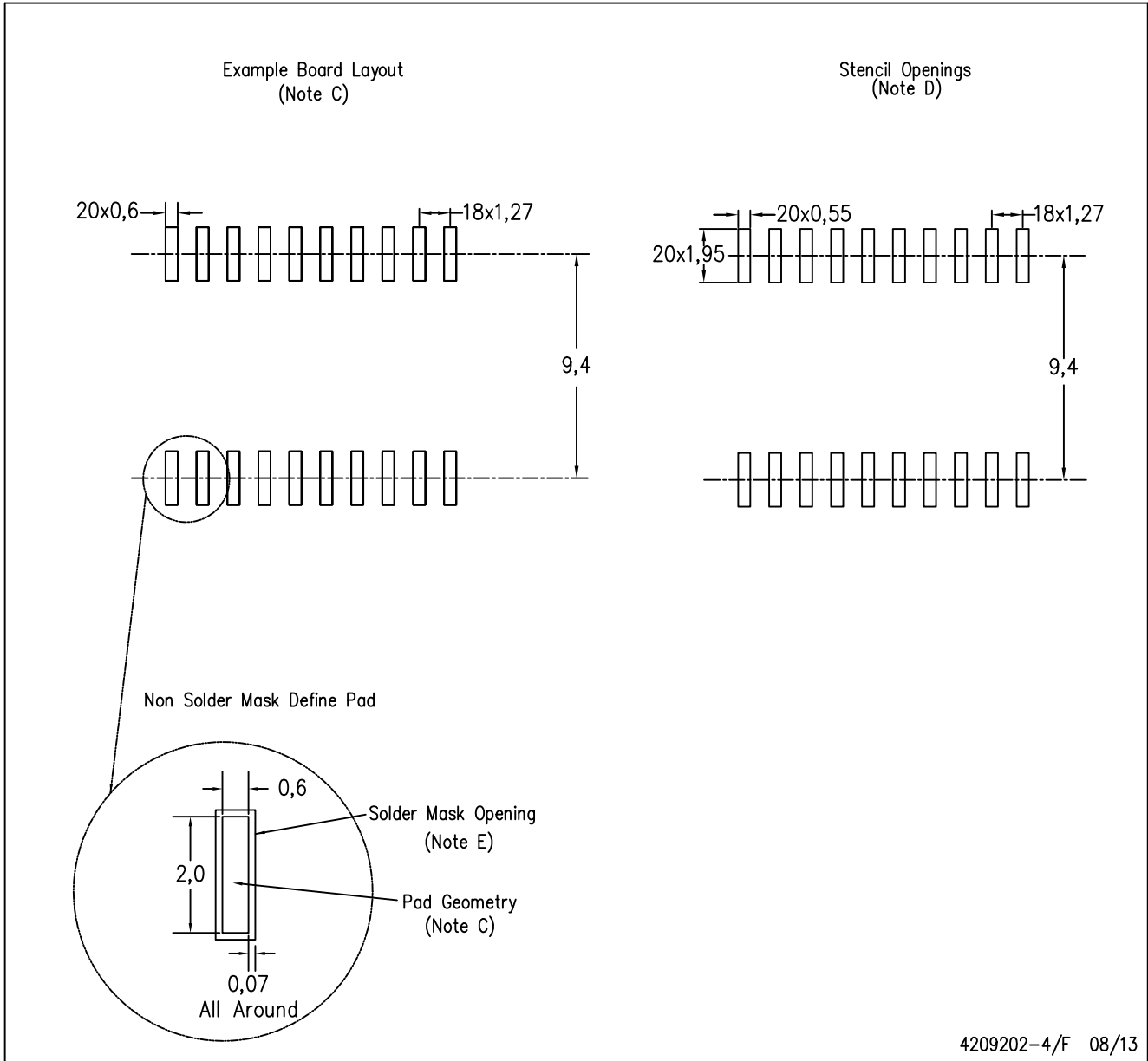
4209202−4/F   08/13

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Refer to IPC7351 for alternate board design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   →   ←   → ‖ ← $\frac{0,30}{0,19}$ ⊕ | 0,10 | Ⓜ

20   11

$\frac{4,50}{4,30}$ Ⓓ $\frac{6,60}{6,20}$

1   10

$\frac{6,60}{6,40}$

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

$\frac{0,75}{0,50}$

1,20 MAX $\frac{0,15}{0,05}$

Seating Plane

◁ | 0,10

4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

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PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/G 08/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM	PINS **	14	16	20	24
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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