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TYPES SN5475, SN5477, SN54L75, SN54L77, SN54LS75, SN54LS77, SN7475, SN74L75, SN74L77, SN74LS75 4-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7611851, MARCH 1974—REVISED OCTOBER 1976

logic

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q ₀	\bar{Q} ₀

H = high level, L = low level, X = irrelevant
Q₀ = the level of Q before the high-to-low transition of G

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The '75, 'L75, and 'LS75 feature complementary Q and \bar{Q} outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77, 'L77, and 'LS77 4-bit latches are available in 14-pin flat packages.

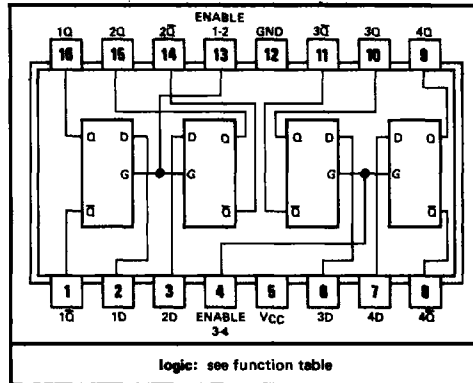
These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54, 54L, and 54LS devices are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, 74L, and 74LS devices are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: '75, 'L75, '77, 'L77	5.5 V
'LS75, 'LS77	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54L', SN54LS' Circuits	-55°C to 125°C
SN74', SN74L', SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

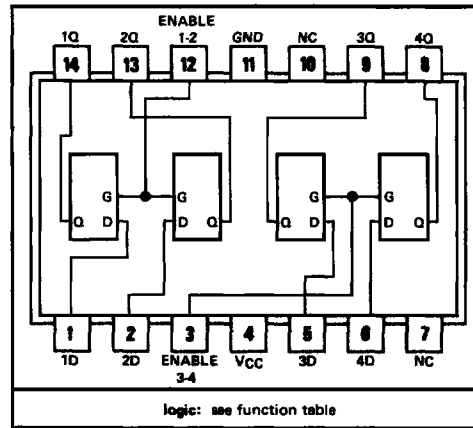
NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

SN5475, SN54LS75 ... J OR W PACKAGE
SN54L75 ... J PACKAGE
SN7475, SN74L75, SN74LS75 ... J OR N PACKAGE
(TOP VIEW)



logic: see function table

SN5477, SN54LS77 ... W PACKAGE
SN54L77, SN74L77 ... T PACKAGE



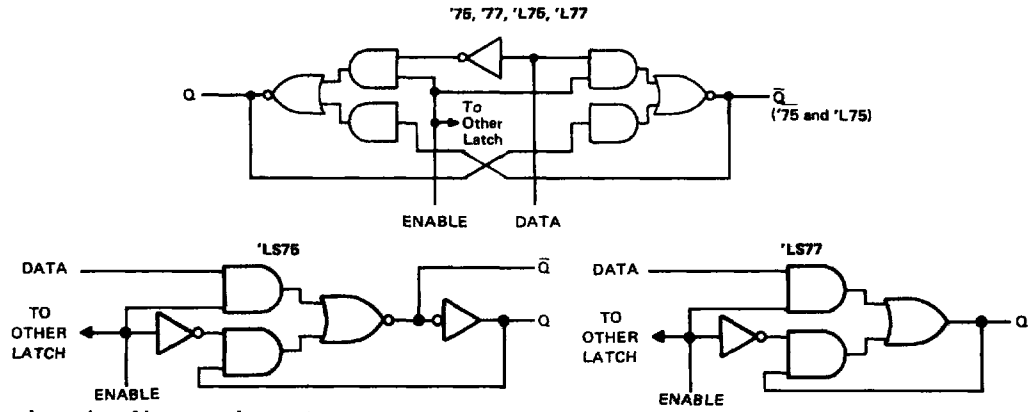
logic: see function table

NC—No internal connection

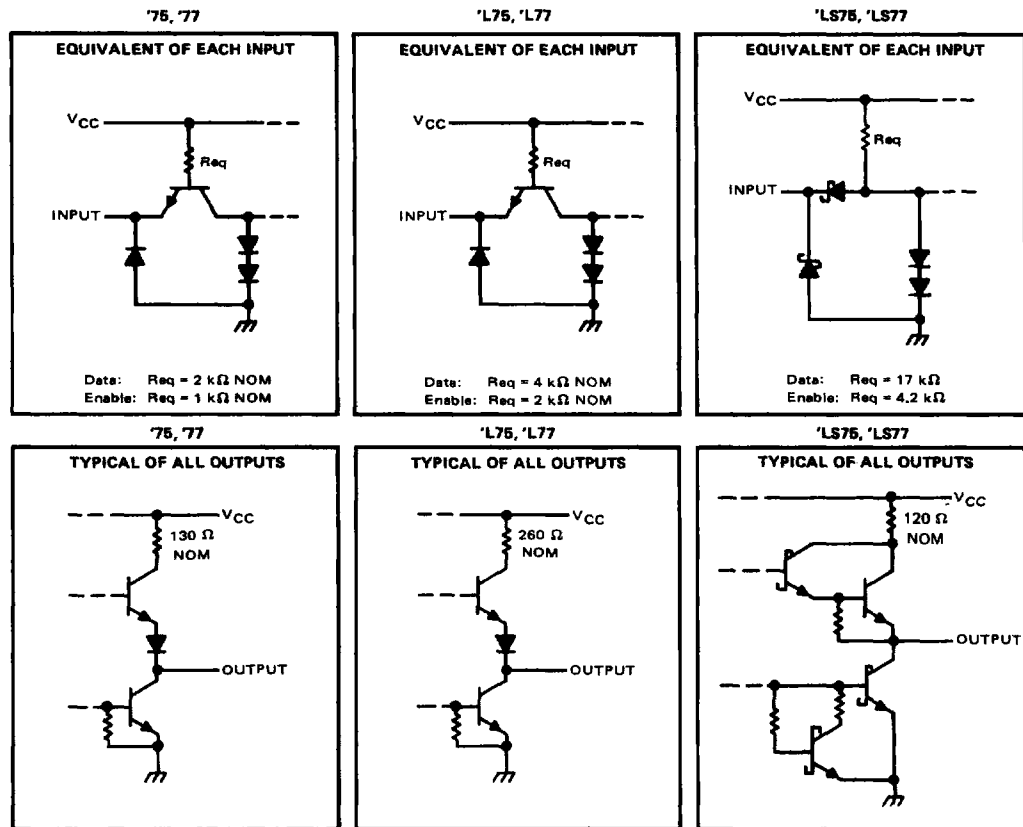
**TYPES SN5475, SN5477, SN54L75, SN54L77, SN54LS75, SN54LS77,
SN7475, SN74L75, SN74L77, SN74LS75**
4-BIT BISTABLE LATCHES

REVISED OCTOBER 1976

functional block diagrams (each latch)



schematics of inputs and outputs



TYPES SN5475, SN5477, SN7475 4-BIT BISTABLE LATCHES

recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	-55	125		0	70		$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	D input			80	μ A
		G input	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$		160	
I_{IL}	Low-level input current	D input			-3.2	mA
		G input	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-6.4	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54 [']	-20	-57	mA
			SN74 [']	-18	-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3	SN54 [']	32	46	mA
			SN74 [']	32	53	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [○]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1		16	30	ns
t_{PHL}					14	25	
t_{PLH}^{\ddagger}	D	\bar{Q}			24	40	ns
t_{PHL}^{\ddagger}					7	15	
t_{PLH}	G	Q			16	30	ns
t_{PHL}					7	15	
t_{PLH}^{\ddagger}	G	\bar{Q}			16	30	ns
t_{PHL}^{\ddagger}					7	15	

[○] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

[‡] These parameters are not applicable for the SN5477.

TYPES SN54L75, SN54L77, SN74L75, SN74L77

4-BIT BISTABLE LATCHES

recommended operating conditions

	SN54L75, SN54L77			SN74L75, SN74L77			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-200			-200	μ A
Low-level output current, I_{OL}			8			8	mA
Width of enabling pulse, t_w	100			100			ns
Setup time, t_{su}	40			40			ns
Hold time, t_h	10			10			ns
Operating free-air temperature, T_A	-65		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN.}$, $I_I = -12 \text{ mA}$			≈ 1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -200 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 8 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX.}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	D input			40	μ A
		G input	$V_{CC} = \text{MAX.}$, $V_I = 2.4 \text{ V}$		80	
I_{IL}	Low-level input current	D input			-1.6	mA
		G input	$V_{CC} = \text{MAX.}$, $V_I = 0.4 \text{ V}$		-3.2	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX.}$	SN54L'	-10	-29	mA
			SN74L'	-9	-29	
I_{CC}	Supply current	$V_{CC} = \text{MAX.}$, See Note 3	SN54L'	16	23	mA
			SN74L'	16	27	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Nor more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [◊]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	$C_L = 15 \text{ pF}$, $R_L = 800 \Omega$, See Figure 1		32	60	ns
t_{PHL}		Q			28	50	
$t_{PLH}\ddagger$	D	\bar{Q}			48	80	ns
$t_{PHL}\ddagger$		\bar{Q}			14	30	
t_{PLH}	G	Q			32	60	ns
t_{PHL}		Q			14	30	
$t_{PLH}\ddagger$	G	\bar{Q}			32	60	ns
$t_{PHL}\ddagger$		\bar{Q}			14	30	

[◊] t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

[‡]These parameters are not applicable for the SN54L77 and SN74L77.

TYPES SN54LS75, SN54LS77, SN74LS75 4-BIT BISTABLE LATCHES

recommended operating conditions

	SN54LS75 SN54LS77			SN74LS75			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_W	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	0			0			ns
Operating free-air temperature, T_A	-55	125		0	70		$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS75 SN54LS77			SN74LS75			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V_{IH} High-level input voltage		2			2			V	
V_{IL} Low-level input voltage				0.7			0.8	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V	
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$			$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	0.25	0.4	0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$					0.1		mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			D input		0.4		0.4	
				G input		20		20	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			D input		80		80	
				G input		-0.4		-0.4	
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$				-20	-100	-20	-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2			'LS75	6.3	12	6.3	12	
				'LS77	6.9	13			

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [◊]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75			'LS77			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D	Q	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figure 1	15	27		11	19		ns
t_{PHL}				9	17		9	17		
t_{PLH}	D	\bar{Q}		12	20					ns
t_{PHL}				7	15					
t_{PLH}	G	Q		15	27		10	18		ns
t_{PHL}				14	25		10	18		
t_{PLH}	G	\bar{Q}		16	30					ns
t_{PHL}				7	15					

[◊] t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

**TYPES SN5475, SN5477, SN54L75, SN54L77, SN54LS75, SN54LS77,
SN7475, SN74L75, SN74L77, SN74LS75**
4-BIT BISTABLE LATCHES

PARAMETER MEASUREMENT INFORMATION

switching characteristics

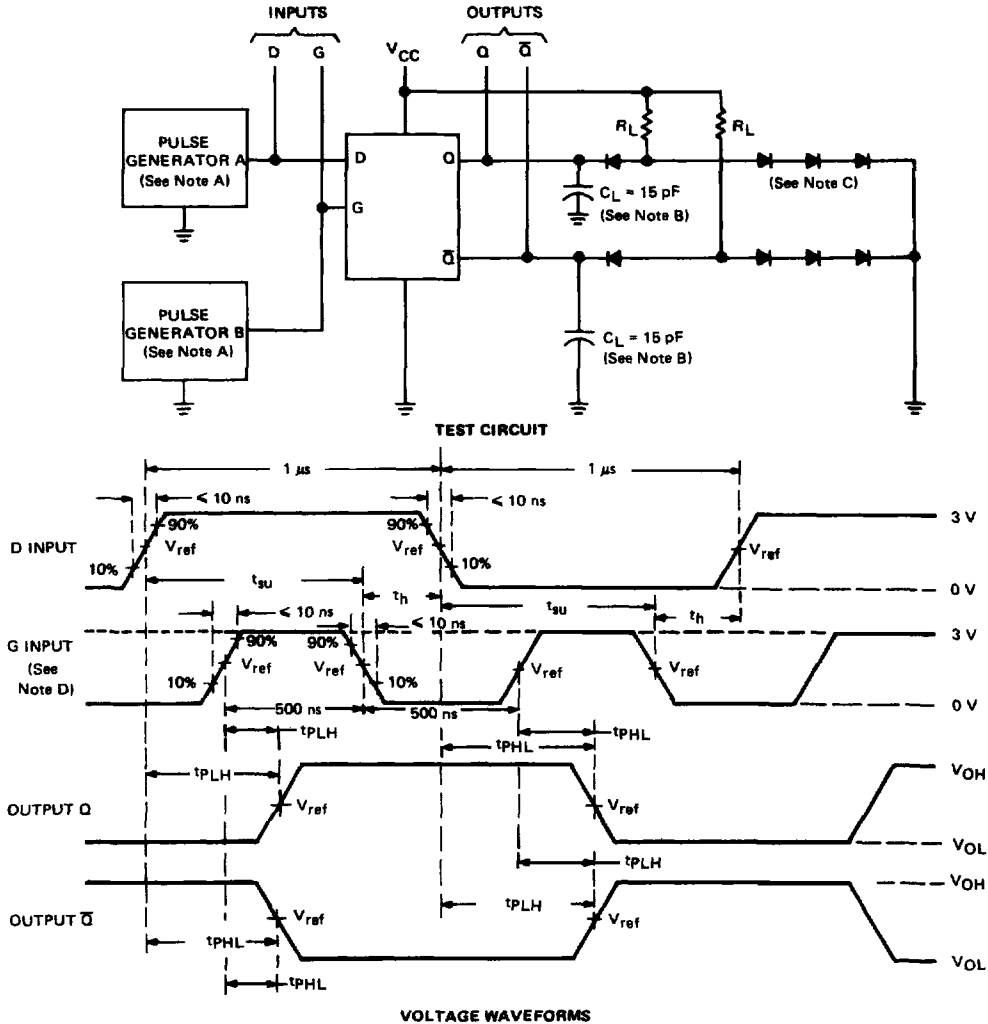


FIGURE 1