PRECISION 1:8 LVPECL FANOUT BUFFER WITH 2:1 RUNT PULSE ELIMINATOR INPUT MUX

Precision Edge® SY89837U

FEATURES

- Selects between two clocks, and provides 8 precision, low skew LVPECL output copies
- Guaranteed AC performance over temperature and supply voltage:
- Wide operating frequency: 1kHz to >1.5GHz
  - <975ps in-to-out t_{pd}
  - <180ps t_r/t_f
  - <40ps output-to-output skew
- Unique input isolation design minimizes crosstalk
- Ultra-low jitter design:
  - <1ps$_{rms}$ random jitter
  - <1ps$_{rms}$ cycle-to-cycle jitter
  - <10ps$_{pp}$ total jitter (clock)
  - <0.7ps$_{rms}$ MUX crosstalk induced jitter
- Unique input termination and VT pin accepts DC- or AC-coupled inputs (CML, PECL, LVDS)
- 800mV LVPECL output swing
- Power supply +2.5V ±5% or +3.3V ±10%
- –40°C to +85°C industrial temperature range
- Available in 32-pin (5mm × 5mm) MLF™ package

APPLICATIONS

- Redundant clock distribution
- Fail-safe clock protection

Precision Edge®

DESCRIPTION

The SY89837U is a low jitter, low skew, high-speed 1:8 fanout buffer with a unique, 2:1 differential input multiplexer (MUX) optimized for clock redundant switchover applications. Unlike standard multiplexers, the SY89837U unique 2:1 runt pulse eliminator (RPE) input MUX prevents any short cycles or "runt" pulses during switchover. In addition, a unique fail-safe input protection prevents metastable conditions when the selected input clock fails to a static DC differential voltage (differential input voltage drops below 200mV). The SY89837U distributes clock frequencies from 1kHz to 1.5GHz, guaranteed, over temperature and voltage.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 200mV without any level shifting or termination resistor networks in the signal path. The outputs are 800mV, 100k compatible LVPECL with fast rise/fall times guaranteed to be less than 200ps.

The SY89837U operates from a +2.5V ±5% or +3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89837U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.

TYPICAL APPLICATIONS CIRCUIT

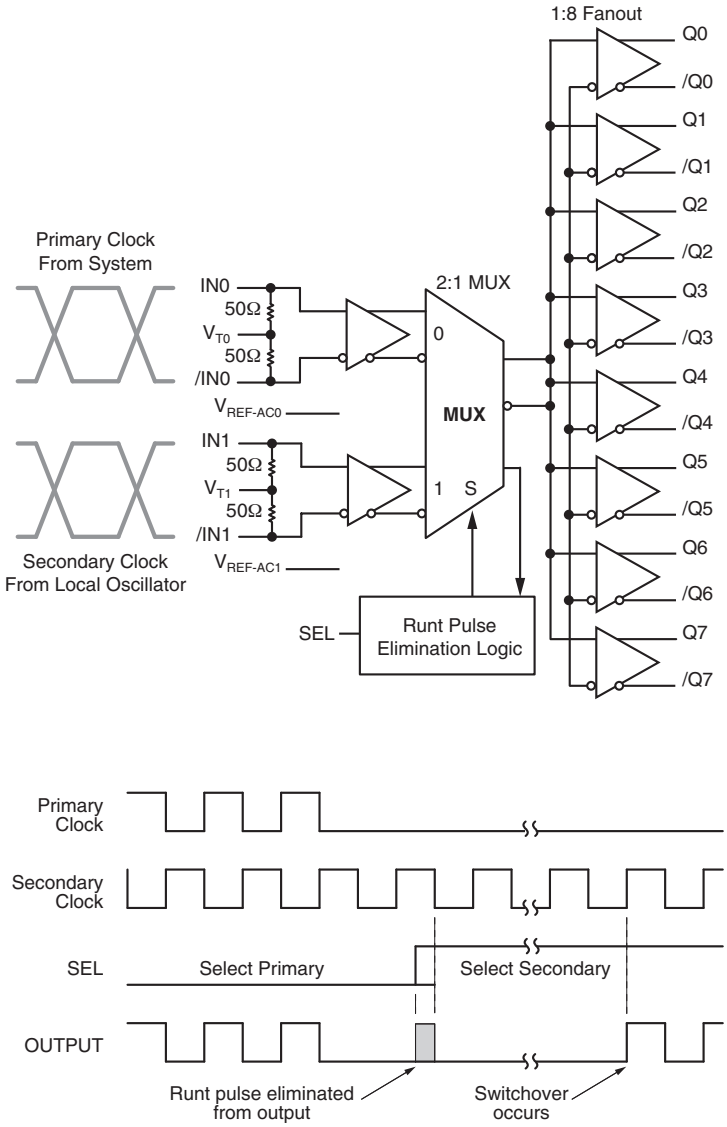
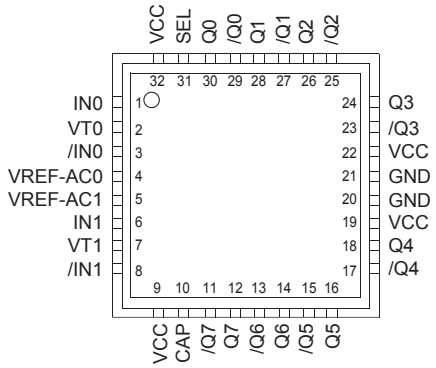


Figure 1. Simplified Example Illustrating Runt Pulse Eliminator (RPE) Circuit When Primary Clock Fails

TRUTH TABLE

Inputs					Outputs	
IN0	**/IN0**	**IN1**	**/IN1**	**SEL**	**Q**	**/Q**
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

PACKAGE/ORDERING INFORMATION



32-Pin MLF™ (MLF-32)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89837UMI	MLF-32	Industrial	SY89837U	Sn-Pb
SY89837UMITR[2]	MLF-32	Industrial	SY89837U	Sn-Pb
SY89837UMG[3]	MLF-32	Industrial	SY89837U with Pb-Free bar-line indicator	Pb-Free NiduAu
SY89837UMGTR[2, 3]	MLF-32	Industrial	SY89837U with Pb-Free bar-line indicator	Pb-Free NiduAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 3, 6, 8	IN0, /IN0, IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 200mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Please refer to the “Input Interface Applications” section for more details.
2, 7	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. See the “Input Interface Applications” section for more details.
31	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. This input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
9, 19, 22, 32	VCC	Positive power supply. Bypass with 0.1μF||0.01μF low ESR capacitors as close to the pins as possible.
30, 28, 26, 24, 18, 16, 14, 12, 29, 27, 25, 23, 17, 15, 13, 11	Q0 – Q7, /Q0 – /Q7	Differential Outputs: These LVPECL output pairs are the outputs of the device. They are a logic function of the IN0, IN1, and SEL inputs. Please refer to the truth table for details. Unused output pairs may be left open.
20,21	GND, Exposed Pad	Ground. Ground and exposed pad to be tied together to most negative potential of chip.
10	CAP	Power-On Reset (POR) Initialization Capacitor. When using the multiplexer with RPE capability, this pin is tied to a capacitor to V_{CC}. The purpose is to ensure the internal RPE logic starts up in a known state. If this pin is tied to V_{CC}, the RPE function will be disabled and the multiplexer will function as a normal multiplexer. See “Application” section for more details. The CAP pin should never be left open.

DETAILED FUNCTIONAL DESCRIPTION

RPE MUX and Fail-Safe Input

The SY89837U is optimized for clock switchover applications where switching from one clock to another clock without runt pulses (short cycles) is required. It features two unique circuits:

1. Runt-Pulse Eliminator (RPE) Circuit

The RPE MUX provides a "glitchless" switchover between two clocks and prevents any runt pulses from occurring during the switchover transition. The design of both clock inputs is identical (i.e., the switchover sequence and protection is symmetrical for both input pair, IN0 or IN1. Thus, either input pair may be defined as the primary input). If not required, the RPE function can be permanently disabled to allow the switchover between inputs to occur immediately. For more detail on how to disable the RPE function within the MUX, see the "Power-On Reset (POR)" section.

2. Fail-Safe Input (FSI) Circuit

The FSI function provides protection against a selected input pair that drops below the minimum amplitude requirement. If the selected input pair drops sufficiently below the 200mV minimum single-ended input amplitude limit (V_{IN}), or 400mV differentially (Vdiff_IN), the output will latch to the last valid clock state.

RPE and FSI Functionality

The basic operation of the RPE MUX and FSI functionality is described with the following four case descriptions. All descriptions are related to the true inputs and outputs. The primary (or selected) clock is called CLK1, the secondary (or alternate) clock is called CLK2. Due to the totally asynchronous relation of the IN and SEL signals and an additional internal protection against metastability, the number of pulses required for the operations described in cases 1 through 4 can vary within certain limits. Refer to "Timing Diagrams" and "Applications" section for detailed information.

Case #1 Two Normal Clocks and RPE Enabled.

In this case the frequency difference between the two running clocks IN0 and IN1 must not be greater than 1.5:1. For example, if the IN0 clock is 500MHz, the IN1 clock must be within the range of 334MHz to 750MHz.

If the SEL input changes state to select the alternate clock, the switchover from CLK1 to CLK2 will occur in three stages:

- **Stage 1:** The output will continue to follow CLK1 for a limited number of pulses.
- **Stage 2:** The output will remain LOW for a limited number of pulses of CLK2.
- **Stage 3:** The output follows CLK2.

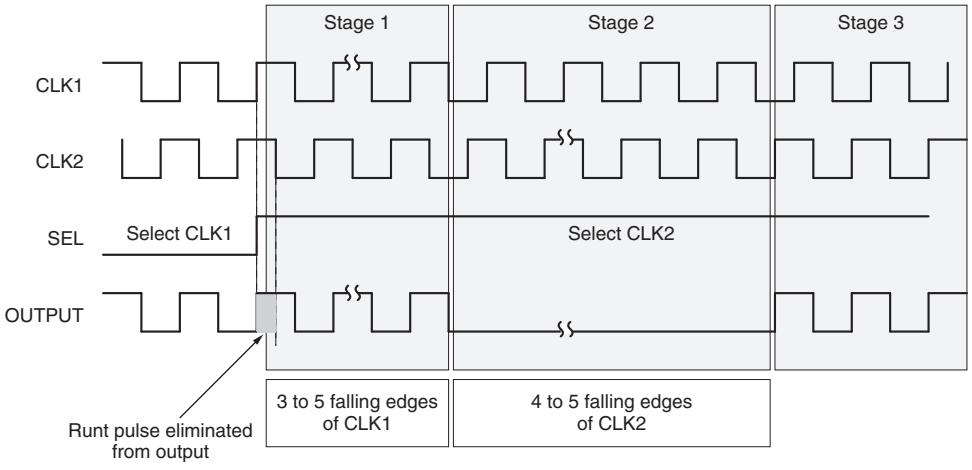


Figure 2. Timing Diagram 1

Case #2 Input Clock Failure: Switching from a selected clock stuck HIGH to a valid clock (RPE enabled).

If CLK1 fails HIGH before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in three stages:

- **Stage 1:** The output will remain HIGH for a limited number of pulses of CLK2.
- **Stage 2:** The output will switch to LOW and then remain LOW for a limited number of falling edges of CLK2.
- **Stage 3:** The output will follow CLK2.

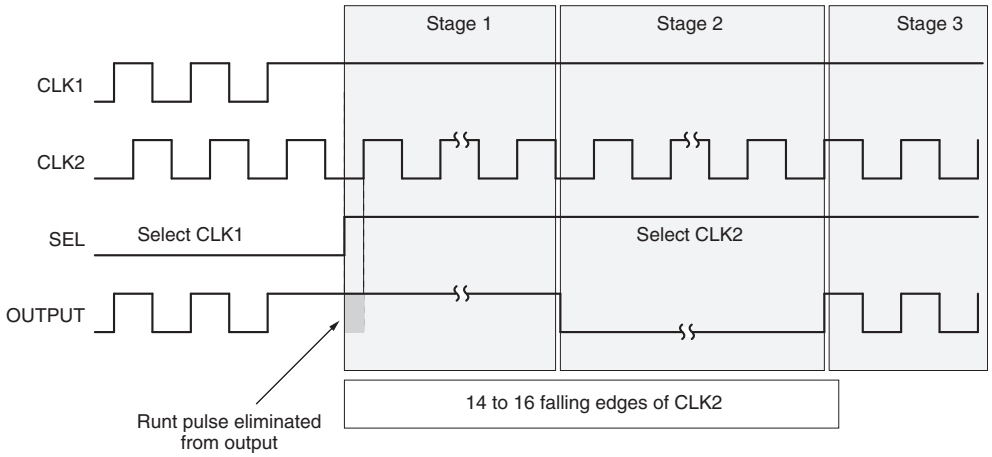


Figure 3. Timing Diagram 2[1]

Note:

1. Output shows extended clock cycle during switchover. Pulse width for both high and low of this cycle will always be greater than 50% of the CLK2 period.

Case #3 Input Clock Failure: Switching from a selected clock stuck LOW to a valid clock (RPE enabled).

If CLK1 fails LOW before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in two stages.

- **Stage 1:** The output will remain LOW for a limited number of falling edges of CLK2.
- **Stage 2:** The output will follow CLK2.

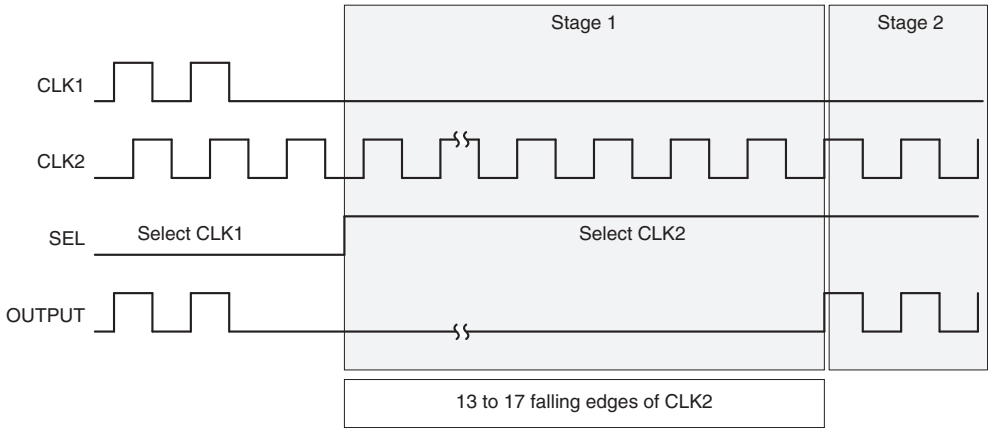


Figure 4. Timing Diagram 3

Case #4 Input Clock Failure: Switching from the selected clock input stuck in an undetermined state to a valid clock input (RPE enabled).

If CLK1 fails to an undetermined state (e.g., amplitude falls below the 200mV (V_{IN}) minimum single-ended input limit, or 400mV differentially) before the RPE MUX selects CLK2 (using the SEL pin), the switchover to the valid clock CLK2 will occur either following Case #2 or Case #3, depending upon the last valid state at the CLK1.

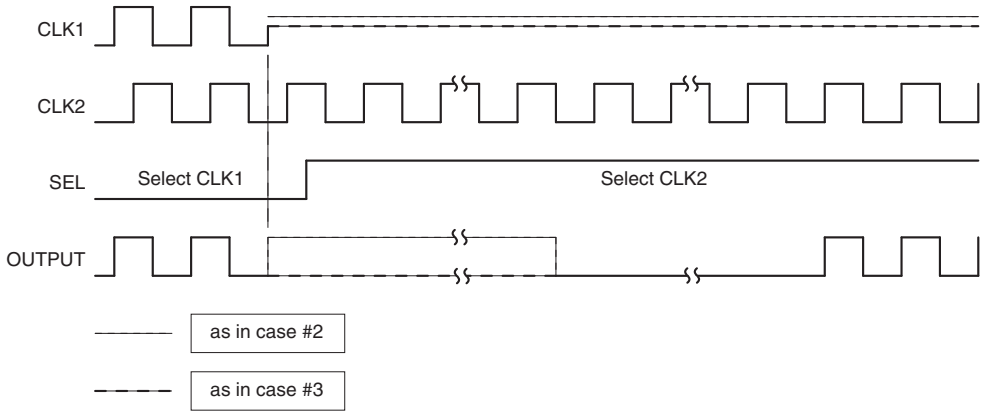


Figure 4. Timing Diagram 4

If the selected input clock fails to a floating, static, or extremely low signal swing, including 0mV, the FSI function will eliminate any metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Please note that the FSI function will not prevent duty cycle distortions or runt pulses in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend upon rise and fall time of the input signal and on its amplitude. Refer to "Operation Characteristics" for detailed information.

POWER-ON RESET (POR) DESCRIPTION

The SY89837U includes an internal power-on reset (POR) function to ensure the RPE logic starts-up in a known logic state once the power-supply voltage is stable. An external capacitor connected between V_{CC} and the CAP pin (pin 10) controls the delay for the power-on reset function.

Calculation of the required capacitor value is based on the time the system power supply needs to power up to a minimum of 2.3V. The time constant for the internal power-on-reset must be greater than the time required for the power supply to ramp up to a minimum of 2.3V.

The following term describes this relationship:

$$C(\mu F) > \frac{tdPS(ms)}{12(ms/\mu F)}$$

As an example, if the time required for the system power supply to power up past 2.3V is 12ms, the required capacitor value on pin 10 would:

$$C(\mu F) > \frac{12ms}{12(ms/\mu F)}$$

$$C > 1\mu F$$

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Volage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Termination Current[3]
  Source or sink current on V_T ..... ±100mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
  MLF™ (θ_{JA})
    Stll-Air ..... 35°C/W
  MLF™ (Ψ_{JB})
    Junction-to-board ..... 16°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A = –40°C to +85°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	2.5V nominal	2.375		2.625	V
		3.3V nominal	3.0		3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		115	160	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN-to-/IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN-to-/IN)		0		V_{IH}–0.2	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a.[6]	0.2		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN–/IN|	See Figure 1b.	0.4			V
V_{IN_LOS}	Input Voltage Swing when signal is lost			100	200	mV
V_{T_IN}	IN-to-V_T (IN-to-/IN)				1.8	V
V_{REF_AC}	Output Reference Voltage (V_{REF}-AC)		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. y_{JB} uses a 4-layer q_{JA} in still air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN} (max.) is specified when V_T is floating.

LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = +2.5V ±5% or +3.3V ±10%; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	500	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1100	1600		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = +2.5V ±5% or +3.3V ±10%; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

Notes:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	RPE enabled	1.5	2.0		GHz
t_{pd}	Differential Propagation Delay IN-to-Q	t_r, t_f (IN) = 300ps (20% to 80%), **Note 9**	525	700	975	ps
	SEL-to-Q	RPE enabled, see Timing Diagram.			17	cycles
	SEL-to-Q	RPE disabled (V_{IN} = V_{CC}/2)			1000	ps
t_{pd} tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{SKEW}	Output-to-output Skew	**Note 10**		20	40	ps
	Part-to-part Skew	**Note 11**			200	ps
t_{JITTER}	Clock Random Jitter (RJ)	**Note 12**			1	ps_{RMS}
	Cycle-to-Cycle Jitter	**Note 13**			1	ps_{RMS}
	Total Jitter (TJ)	**Note 14**			10	ps_{PP}
	Crosstalk-Induced Jitter	**Note 15**			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	70	120	180	ps

Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Propagation delay is a function of rise and fall time at IN. See “Operation Characteristics” for more details.
10. Output-to-output skew is measured between two different outputs under identical transitions.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
12. Random jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

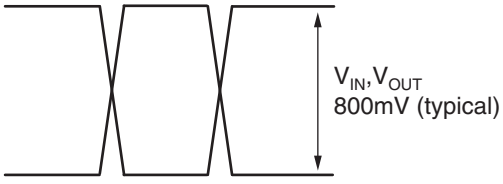


Figure 1a. Simplified Differential Input Swing

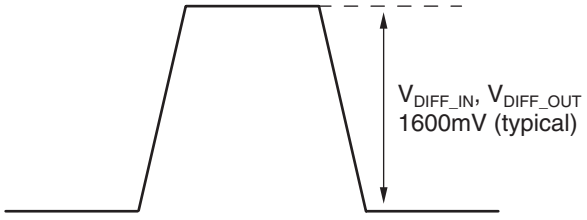
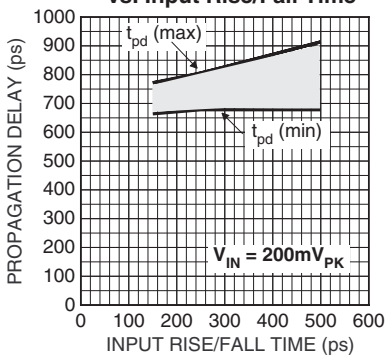


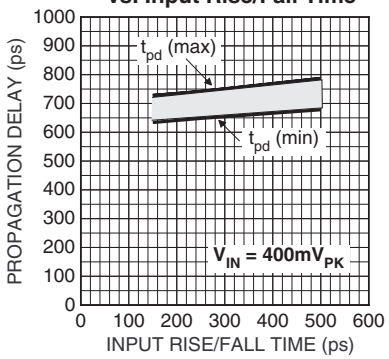
Figure 1b. Simplified LVPECL Output Swing

OPERATING CHARACTERISTICS

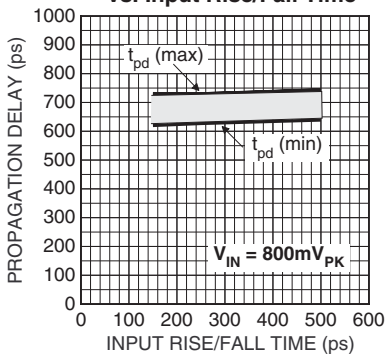
Propagation Delay Variation vs. Input Rise/Fall Time



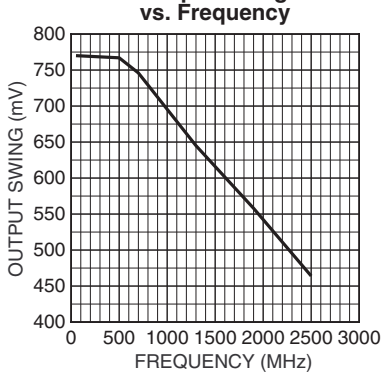
Propagation Delay Variation vs. Input Rise/Fall Time



Propagation Delay Variation vs. Input Rise/Fall Time

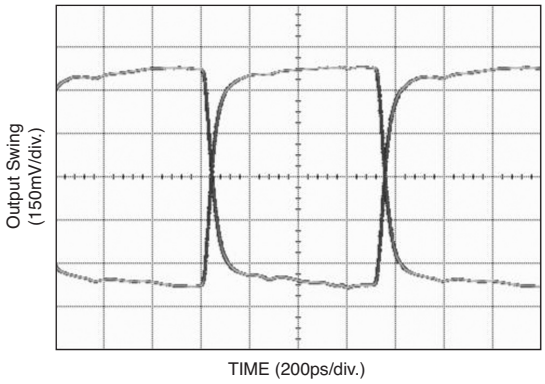


Output Swing vs. Frequency

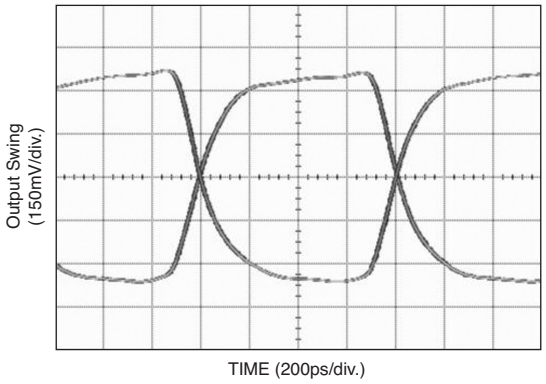


OPERATING CHARACTERISTICS (CONTINUED)

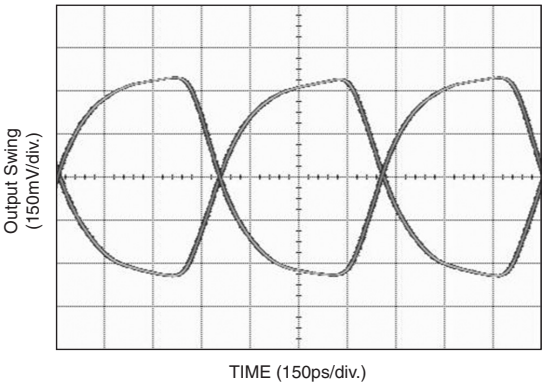
200MHz Clock



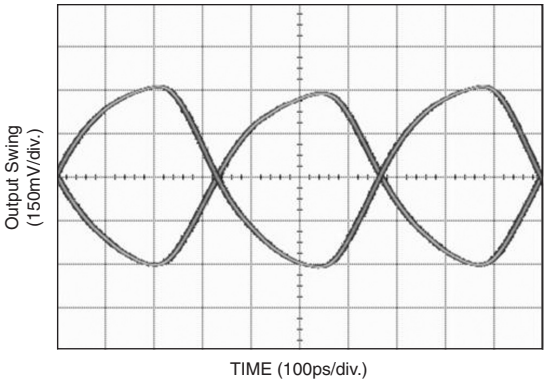
622MHz Clock



1GHz Clock



1.5GHz Clock



INPUT AND OUTPUT STAGES

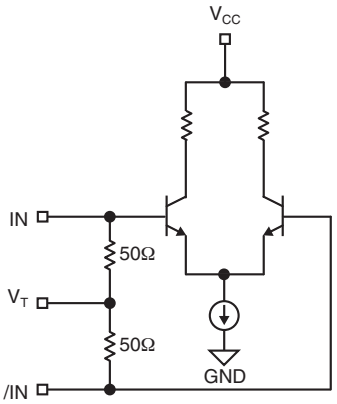


Figure 2a. Simplified Differential Input Stage

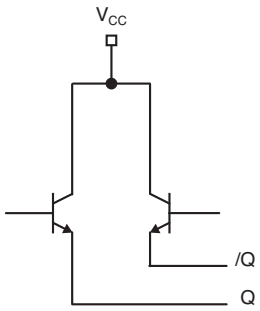
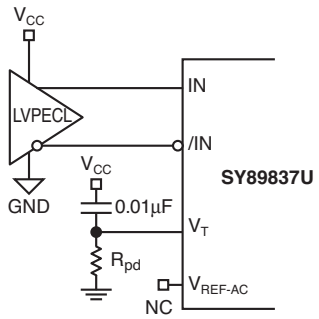


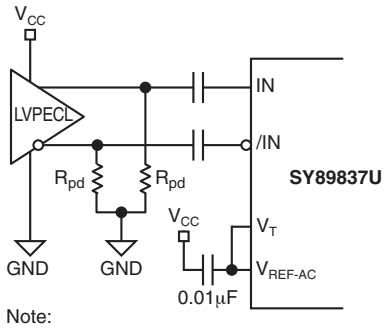
Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS



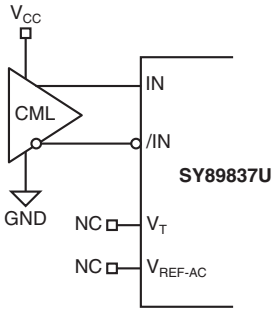
Note:
For 3.3V, R_{pd} = 50Ω.
For 2.5V, R_{pd} = 39Ω.

Figure 3a. LVPECL Interface (DC-Coupled)



Note:
For 3.3V, R_{pd} = 100Ω.
For 2.5V, R_{pd} = 50Ω.

Figure 3b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}.

Figure 3c. CML Interface (DC-Coupled)

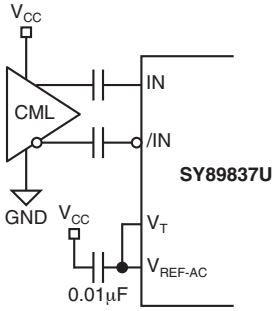


Figure 3d. CML Interface (AC-Coupled)

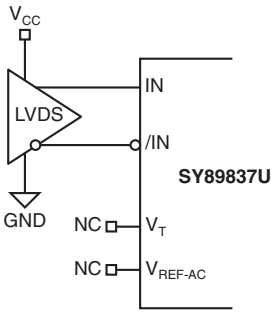


Figure 3e. LVDS Interface

LVPECL OUTPUT INTERFACE APPLICATIONS

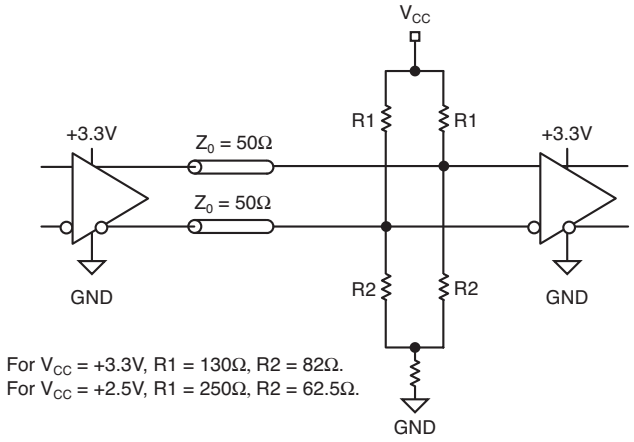


Figure 4a. Parallel Thevenin-Equivalent Termination

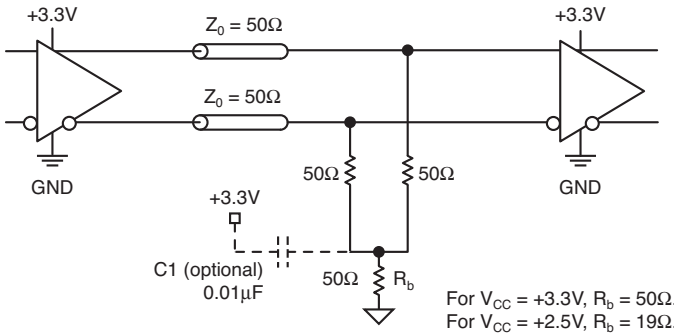
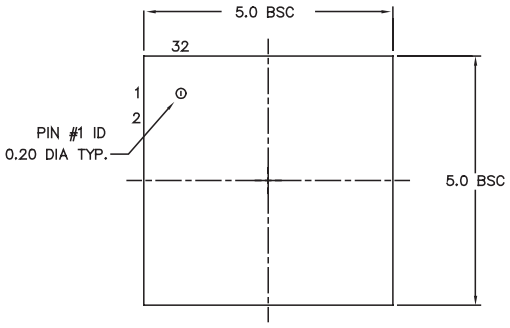


Figure 4b. Parallel Termination (3-Resistors)

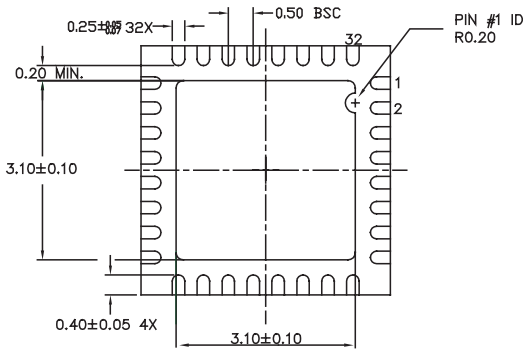
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
	MLF™ Application Note	www.amkor.com/product/notes_papers/MLFAppNote.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

32-PIN *Micro*LeadFrame™ (MLF-32)

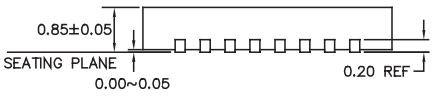


TOP VIEW

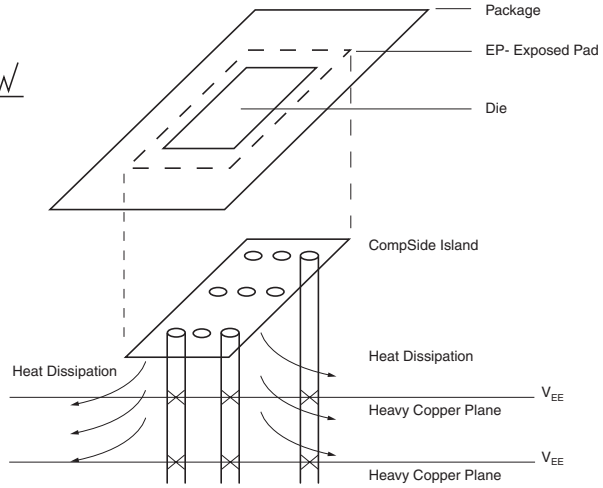


BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW



PCB Thermal Consideration for 32-Pin MLF™ Package

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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