Octal latched transceiver with dual enable (3-State) — 74ABT543

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT543 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 'ABT543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A in-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn	C_L = 50pF; V_{CC} = 5V	4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

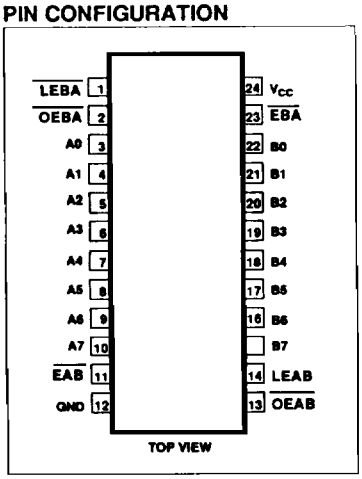
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT543N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT543D

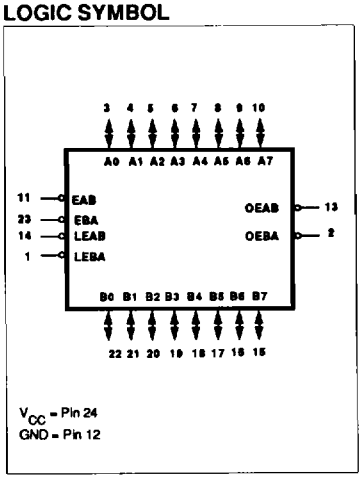
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (Active Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (Active Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (Active Low)
3, 4, 5, 6 7, 8, 9, 10	A0 - A7	Port A, 3-State outputs
22, 21, 20, 19 18, 17, 16, 15	B0 - B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

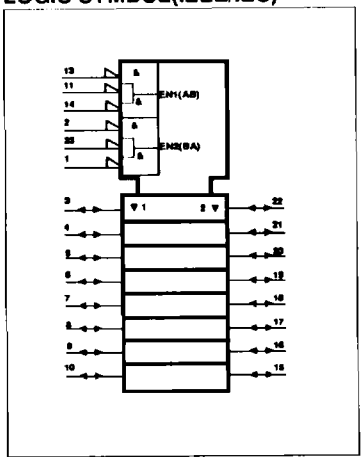
PIN CONFIGURATION



LOGIC SYMBOL

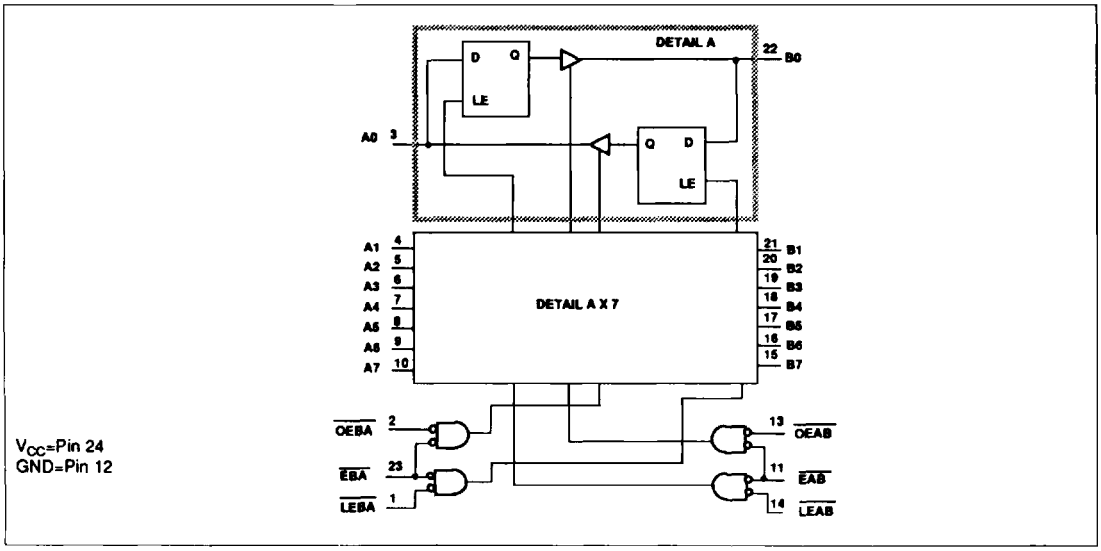


LOGIC SYMBOL(IEEE/IEC)



Octal latched transceiver with dual enable (3-State) 74ABT543

LOGIC DIAGRAM



puts. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE

INPUTS $\overline{OEXX}$	INPUTS $\overline{EXX}$	INPUTS $\overline{LEXX}$	INPUTS DATA	OUTPUTS	STATUS
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC ELECTRICAL CHARACTERISTICS

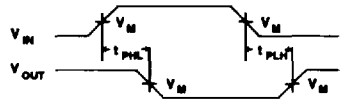
GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = -40°C to +85°C, V_{CC} = 5V±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 2	1.9 1.9	4.4 4.4	5.9 5.9	1.9 1.9	6.9 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	Waveform 1, 2	1.6 2.1	4.1 4.6	5.6 6.1	1.6 2.1	6.6 7.1	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 4 Waveform 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 4 Waveform 5	3.4 3.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	Waveform 4 Waveform 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	Waveform 4 Waveform 5	3.4 3.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns

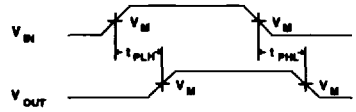
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = -40°C to +85°C, V_{CC} = 5V±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	Waveform 3	3.5 3.0			3.5 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	Waveform 3	0.5 0.5			0.5 0.5		ns
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{EAB}$, Bn to $\overline{EBA}$	Waveform 3	3.5 3.0			3.5 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	Waveform 3	0.5 0.5			0.5 0.5		ns
$t_w(L)$	Latch enable pulse width, Low	Waveform 3	3.5			3.5		ns

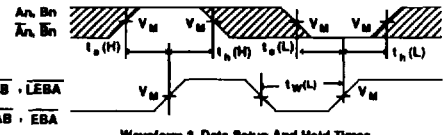
AC WAVEFORMS



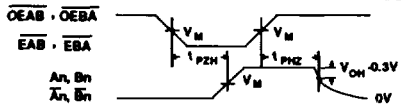
Waveform 1. Propagation Delay For Inverting Output



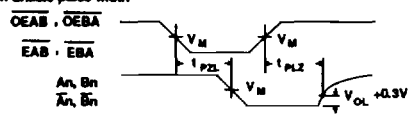
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup And Hold Times And Latch Enable pulse width



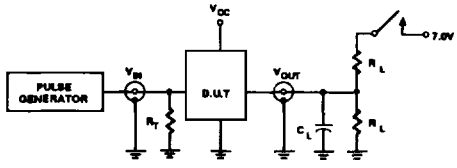
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



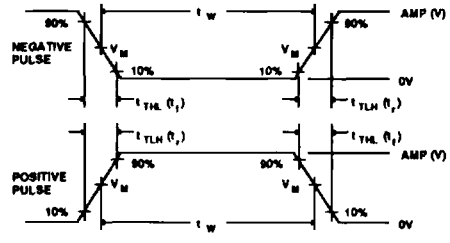
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

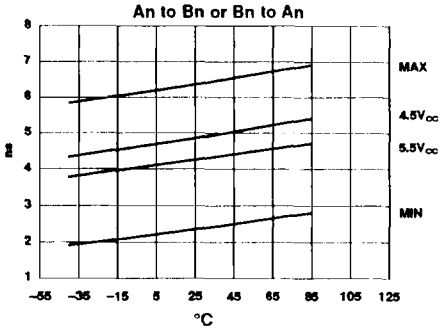
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



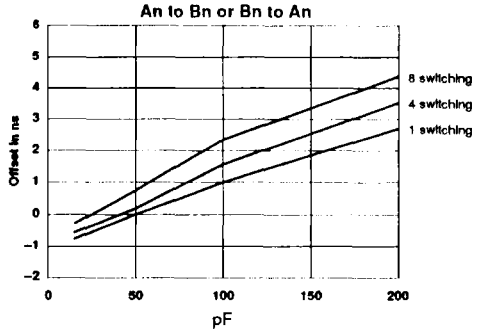
V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

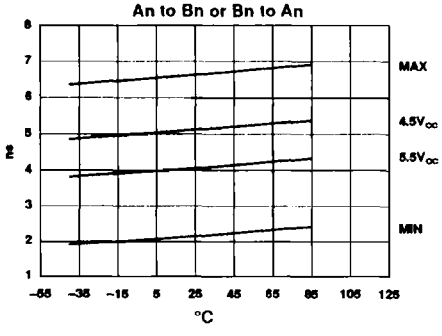
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



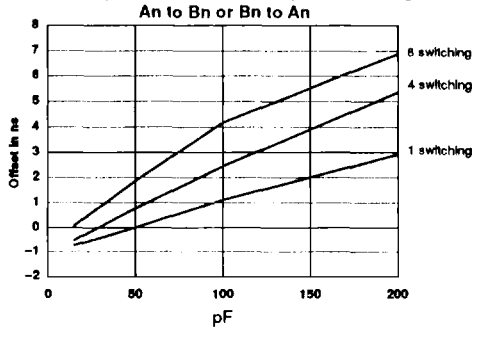
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



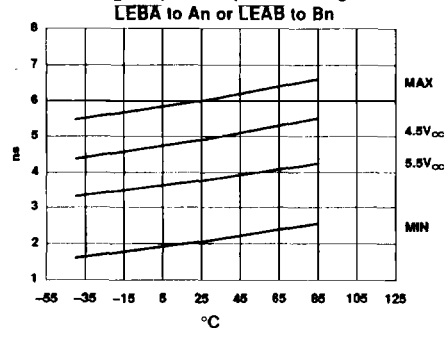
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



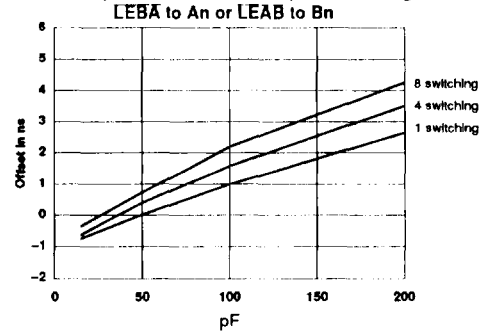
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



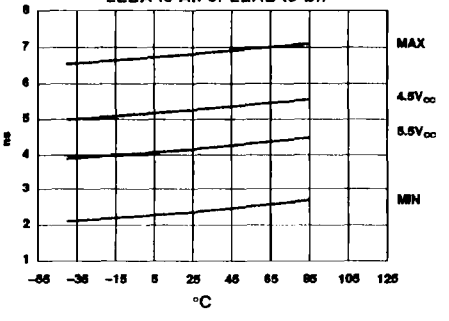
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
LEBA to An or LEAB to Bn



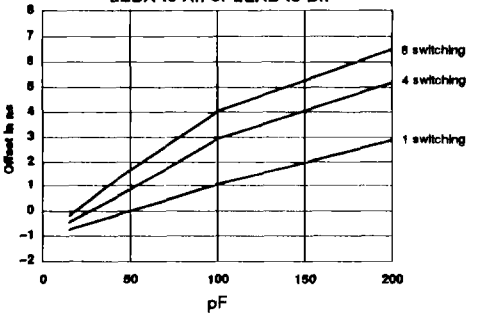
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
LEBA to An or LEAB to Bn



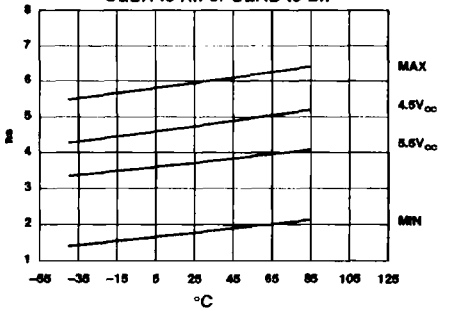
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn



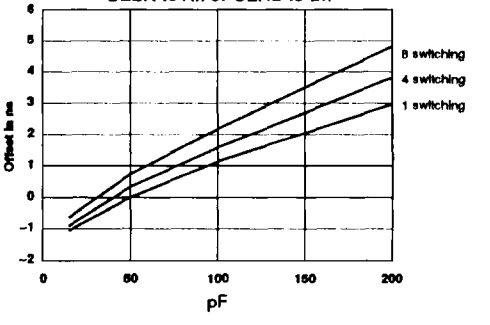
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn



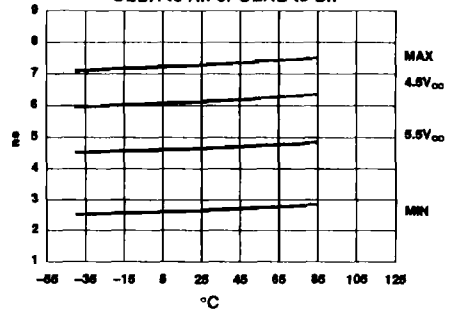
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



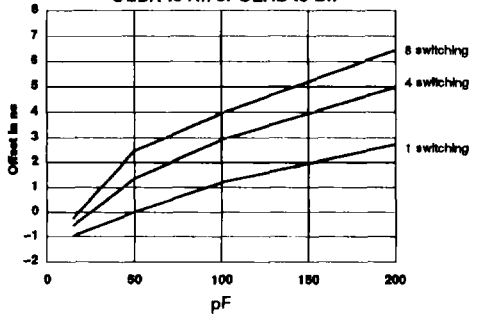
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



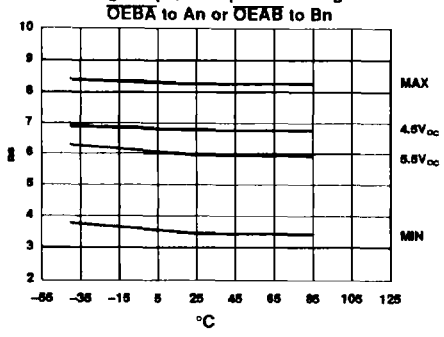
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



Adjustment of t_{PHZ} for
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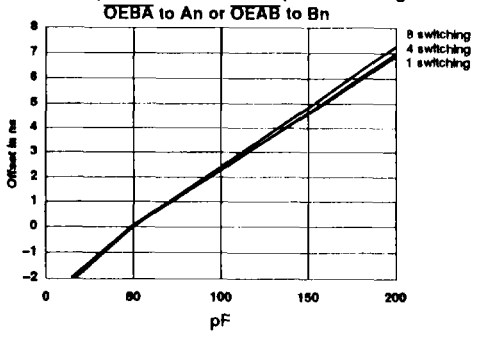
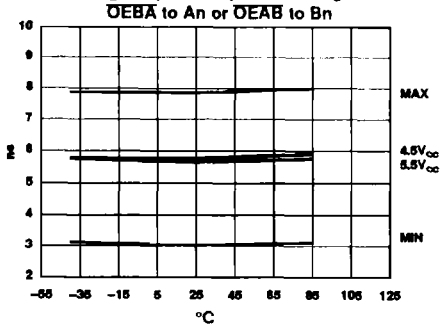
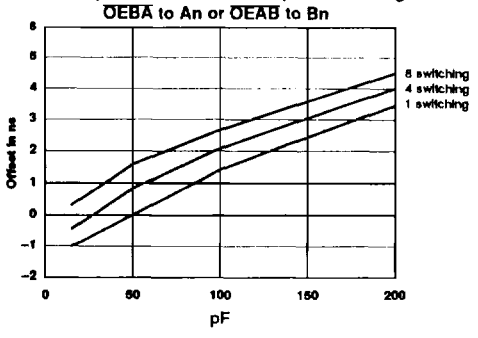
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



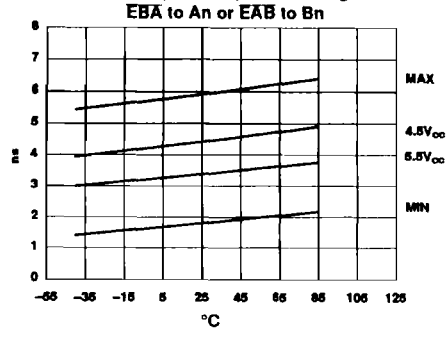
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



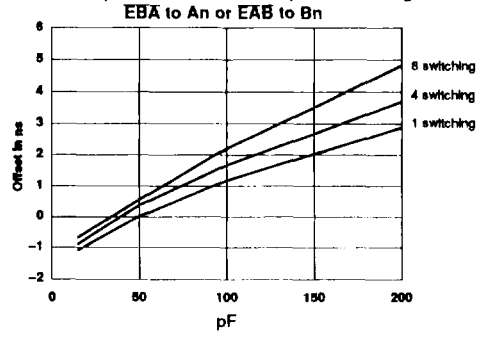
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



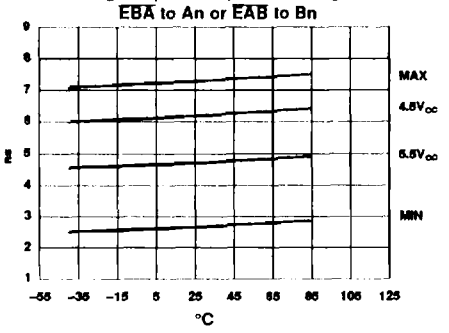
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



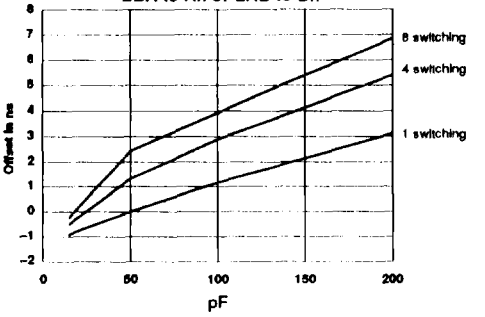
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



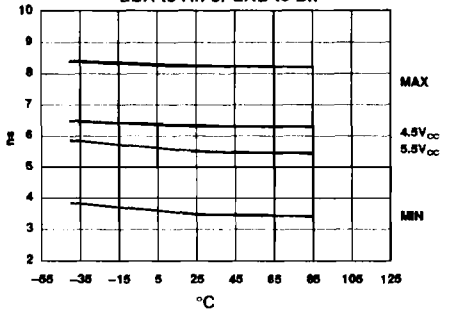
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



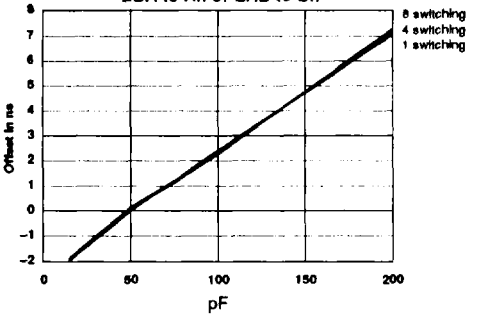
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



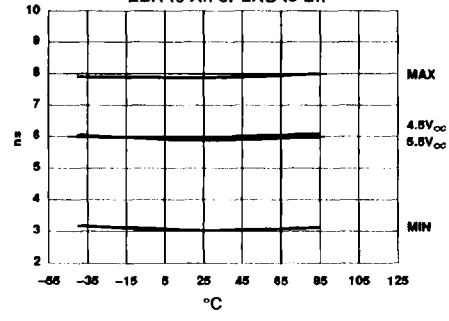
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



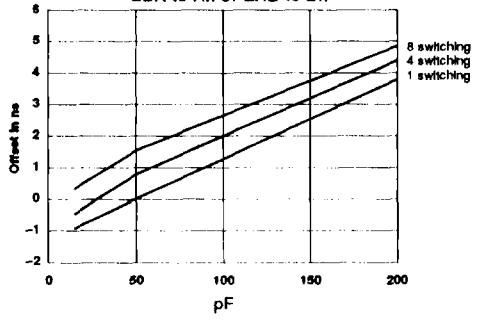
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



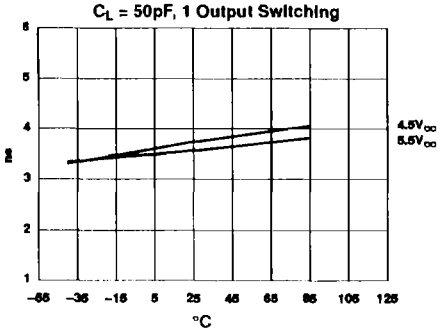
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



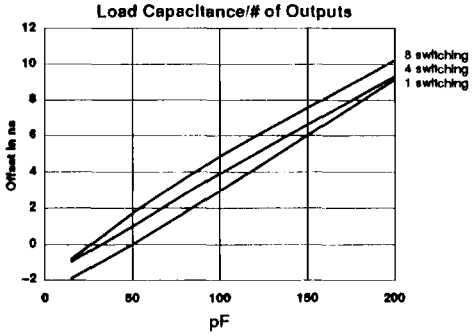
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



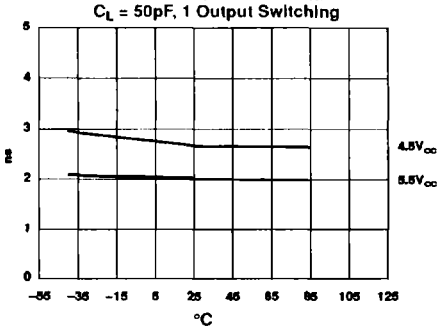
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



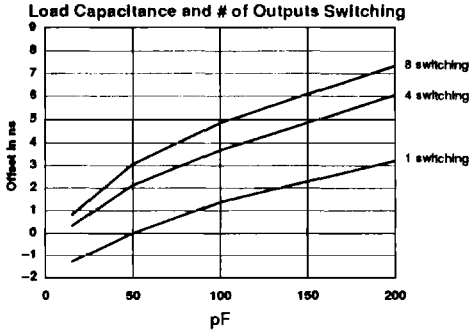
Adjustment of t_{TLH} for
Load Capacitance/# of Outputs



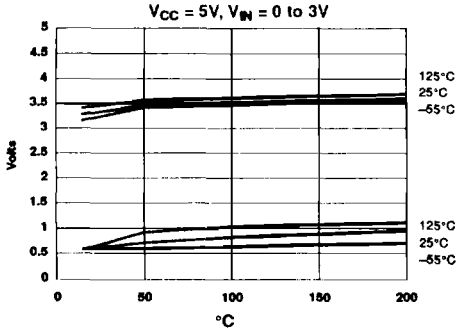
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V