FAST CMOS OCTAL TRANSCEIVER/ REGISTER (3-STATE)

IDT74FCT646AT/CT

FEATURES:

- **A and C grades**
- **Low input and output leakage ≤1µA (max.)**
- **CMOS power levels**
- **True TTL input and output compatibility:**
  - *V_{OH} = 3.3V (typ.)*
  - *V_{OL} = 0.3V (typ.)*
- **High Drive outputs (-15mA I_{OH}, 64mA I_{OL})**
- **Meets or exceeds JEDEC standard 18 specifications**
- **Power off disable outputs permit "live insertion"**
- **Available in SOIC, SSOP, and QSOP packages**

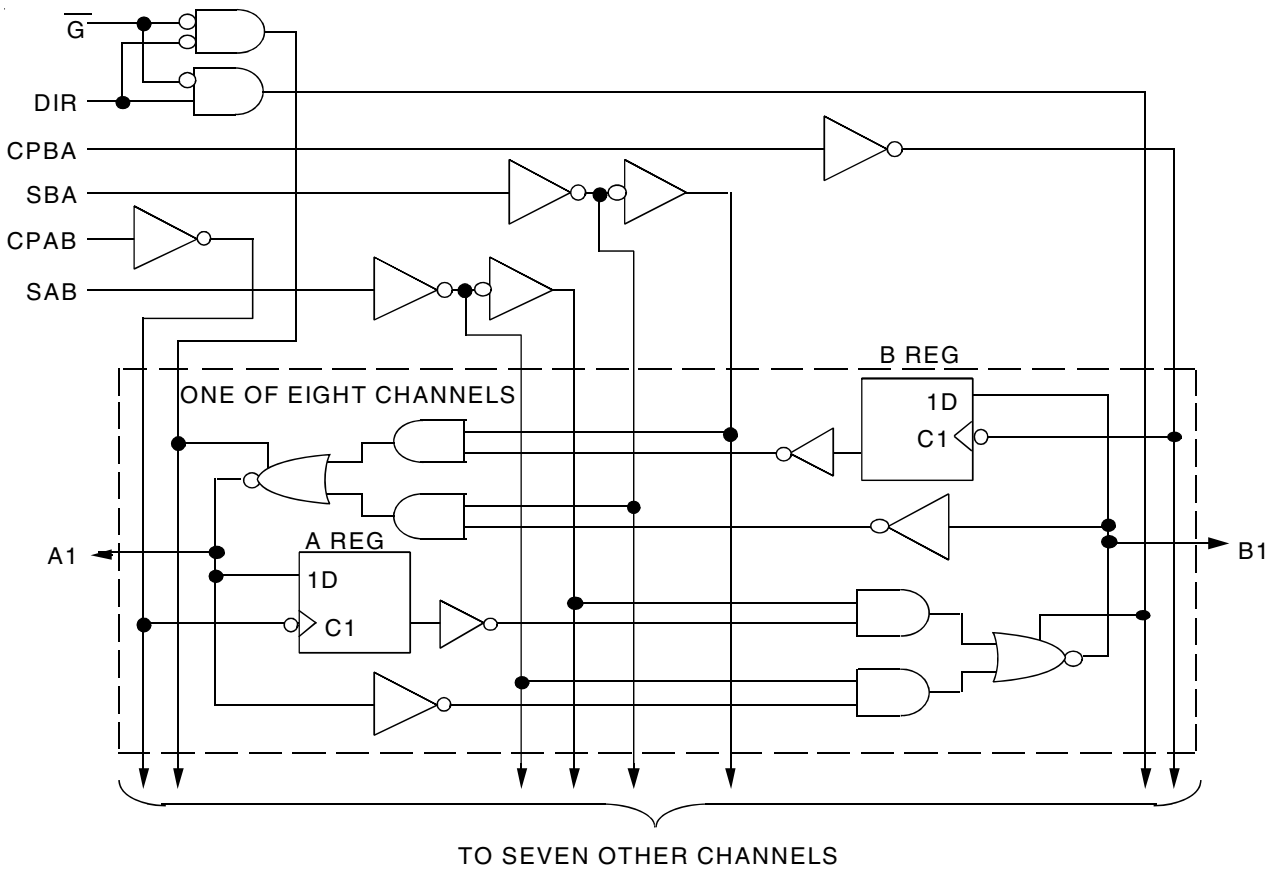
DESCRIPTION:

The FCT646T consists of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The FCT646T utilizes the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

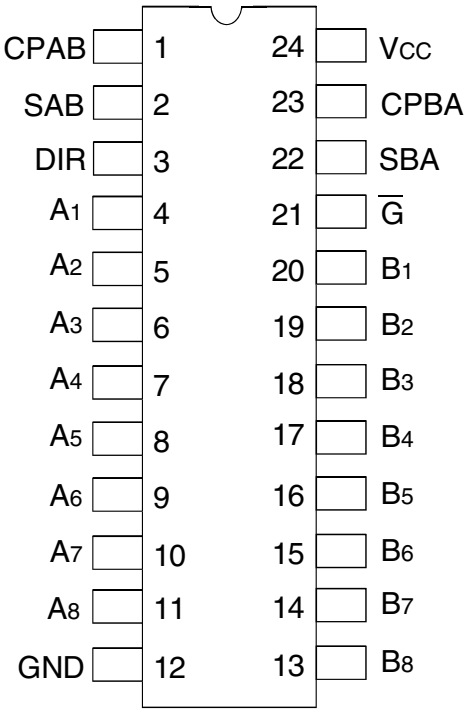
SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
A_1 - A_8	Data Register A Inputs Data Register B Outputs
B_1 - B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs

FUNCTION TABLE[1]

Inputs						Data I/O[2]		Operation or Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

NOTES:
1. H = HIGH
   L = LOW
   X = Don't Care
   ↑ = LOW-to-HIGH transition.
   Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
2. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

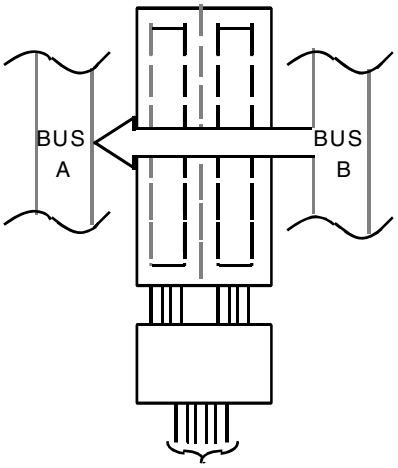
Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	µA

OUTPUT DRIVE CHARACTERISTICS

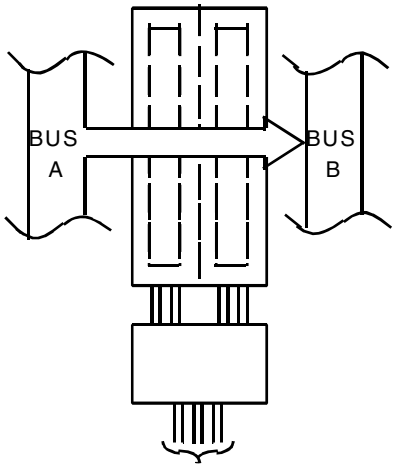
Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = –8mA MIL	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA MIL	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 64mA	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}					
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.



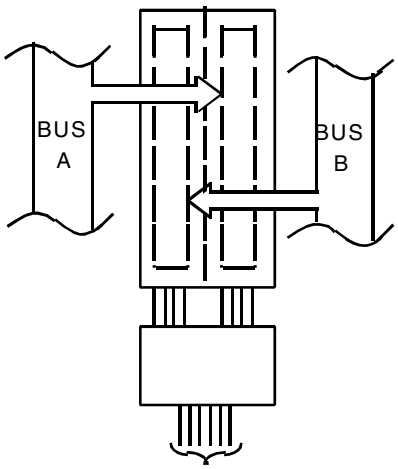
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to A



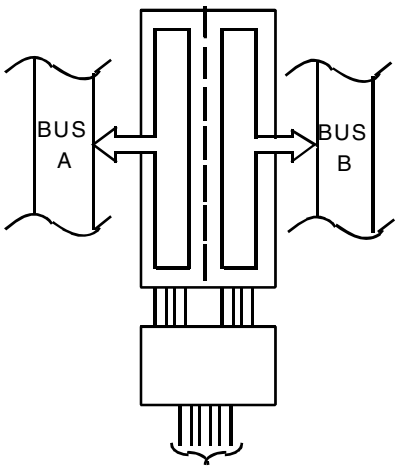
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to B



DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

Storage From
A and/or B



DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stores [1]
Data to A and/or B

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		$\overline{G}$ = DIR = GND One Bit Toggling at fi = 5MHz	V_{IN} = 3.4V V_{IN} = GND	—	2	5.5	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
		$\overline{G}$ = DIR = GND Eight Bits Toggling at fi = 2.5MHz	V_{IN} = 3.4V V_{IN} = GND	—	6	16.3[5]	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Output Frequency
   N_i = Number of Outputs at f_i

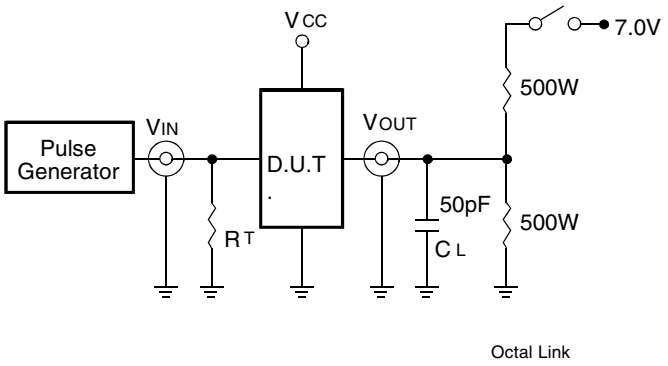
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	54/74FCT646AT		74FCT646CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay, Bus to Bus	C_L = 50pF R_L = 500Ω	2	6.3	1.5	5.4	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{G}$, DIR to Bus		2	9.8	1.5	7.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{G}$, DIR to Bus		2	6.3	1.5	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay, Clock to Bus		2	6.3	1.5	5.7	ns
t_{PLH} t_{PHL}	Propagation Delay, SBA or SAB to Bus		2	7.7	1.5	6.2	ns
t_{SU}	Set-up Time HIGH or LOW, Bus to Clock		2	—	2	—	ns
t_H	Hold Time HIGH or LOW, Bus to Clock		1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		5	—	5	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS



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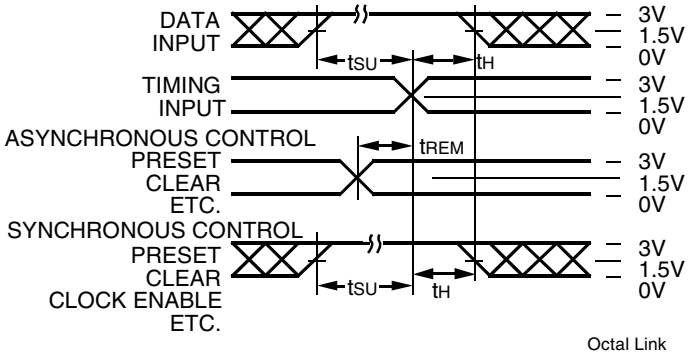
Test Circuits for All Outputs



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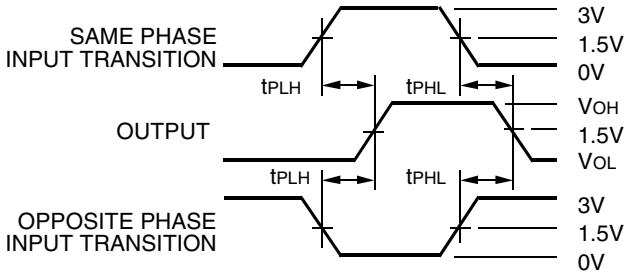
Set-Up, Hold, and Release Times



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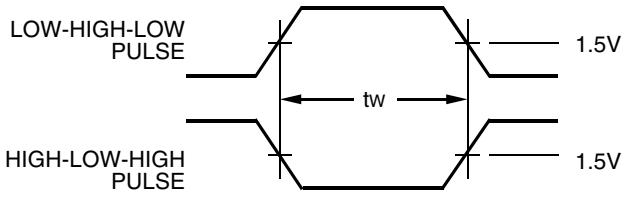
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

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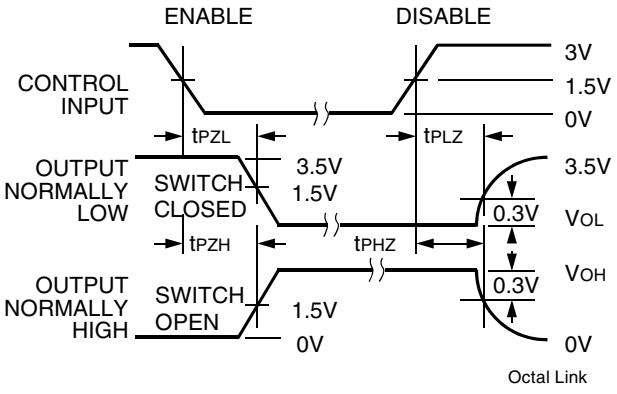

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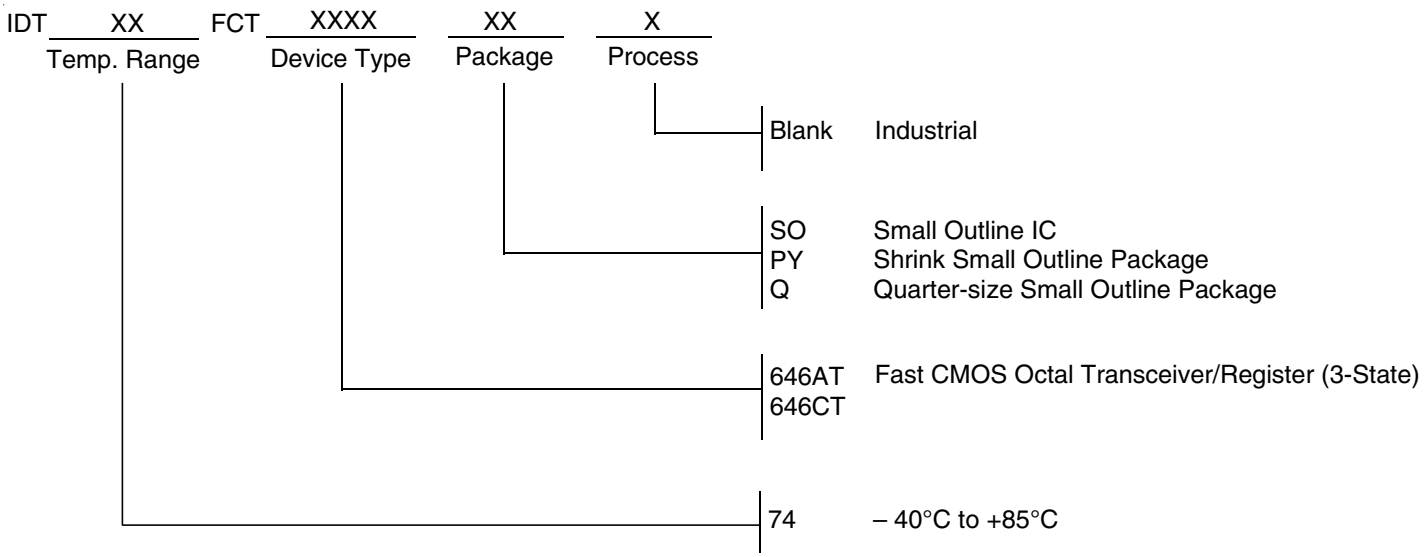
Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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