National Semiconductor

March 1993

74ACTQ652
Quiet Series Transceiver/Register

General Description

The 'ACTQ652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

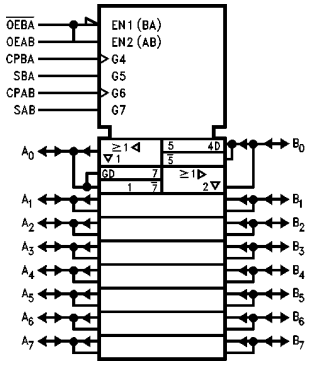
The 'ACTQ652 utilizes NSC's FACT Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Outputs source/sink 24 mA
- TTL-compatible inputs

Logic Symbols

IEEE/IEC



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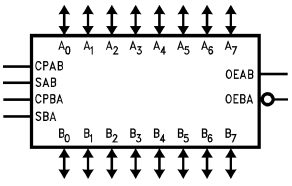

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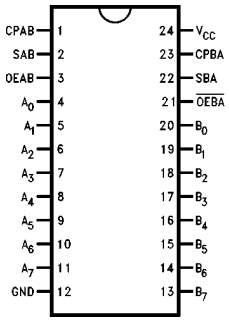
Connection Diagram

Pin Assignment
DIP and SOIC



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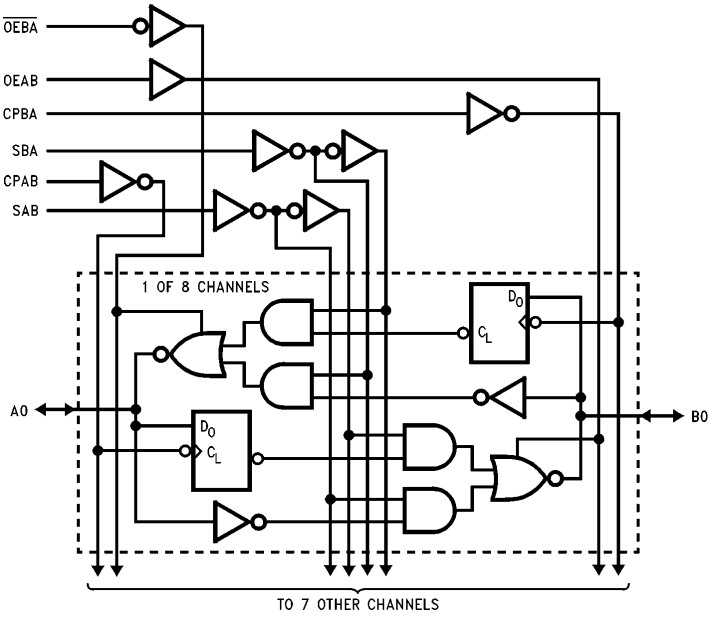
Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

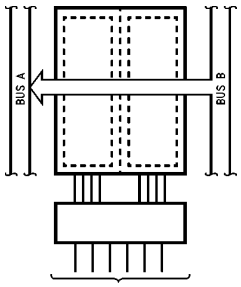
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Note A: Real-Time Transfer Bus B to Bus A



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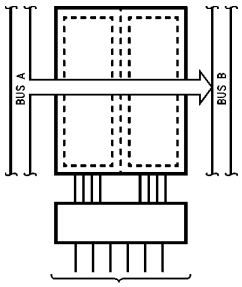
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B



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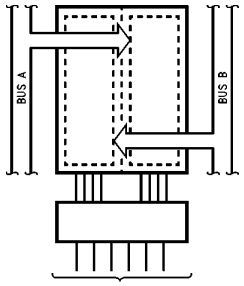
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Note C: Storage



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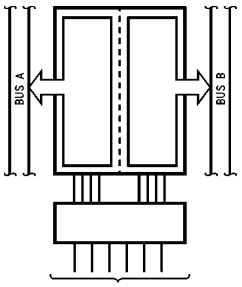
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↗	X	X	X
L	X	X	↗	X	X
L	H	↗	↗	X	X

Note D: Transfer Storage Data to A or B



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OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1

Function Table

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	−40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	*$V_{IN} = V_{IL}$ or V_{IH}
		5.5		4.86	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH}
		5.5		0.36	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±6.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5		V	*Figures 12, 13* (Notes 1, 2)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2		V	*Figures 12, 13* (Notes 1, 2)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Notes 1, 3)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Notes 1, 3)

Note 1: PDIP package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 3: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{max}	Max. Clock Frequency	5.0						MHz
t_{PLH}, t_{PHL}	Propagation Delay Clock to Bus	5.0	2.0	7.0	9.5	2.0	10.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Bus to Bus	5.0	2.0	6.5	9.0	2.0	9.5	ns
t_{PLH}, t_{PHL}	Propagation Delay SBA or SAB to A or B	5.0	2.5	6.5	10.0	2.5	10.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PZH}, t_{PZL}	Enable Time *OEBA to A	5.0	2.0	7.0	10.5	2.0	11.0	ns
t_{PHZ}, t_{PLZ}	Disable Time *OEBA to A	5.0	1.0	5.0	8.0	1.0	8.5	ns
t_{PZH}, t_{PZL}	Enable Time OEAB to B	5.0	2.0	7.0	10.5	2.0	11.0	ns
t_{PHZ}, t_{PLZ}	Disable Time OEAB to B	5.0	1.0	5.0	8.0	1.0	8.5	ns
$t_s(H)$, $t_s(L)$	Setup Time, HIGH or LOW, Bus to Clock	5.0	3.0			3.0		ns
$t_h(H)$, $t_h(L)$	Hold Time, HIGH or LOW, Bus to Clock	5.0	1.5			1.5		ns
$t_w(H)$, $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0	4.0			4.0		ns
t_{OSHL}, t_{OSLH}	Output to Output Skew** A to B, B to A or Clock to Output	5.0		0.5	1.0		1.0	ns

*Voltage range is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any separate outputs of the same device. The specification applies to any output switching in the same direction, either HIGH to LOW (T_{OSHL}) or LOW to HIGH (T_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	54	pF	$V_{CC} = 5.0V$

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the work generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

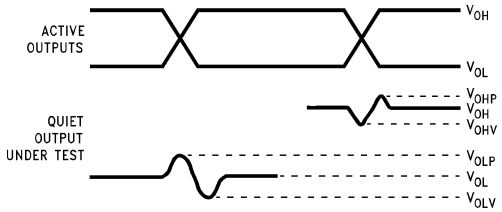

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FIGURE 2. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, $t_r = 3$ ns, $t_f = 3$ ns, skew < 150 ps.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

FACT Noise Characteristics (Continued)

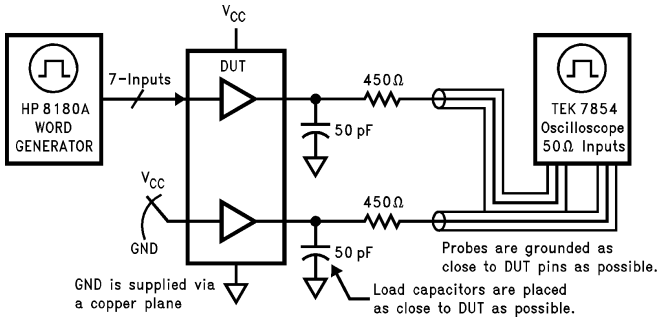

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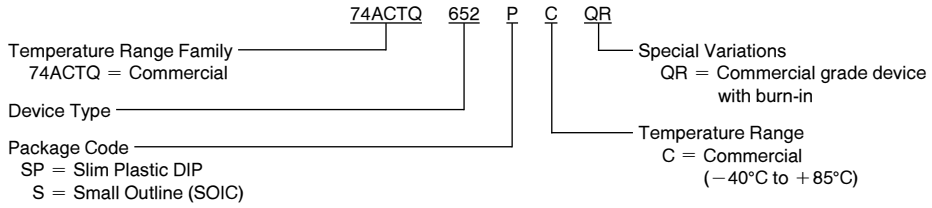
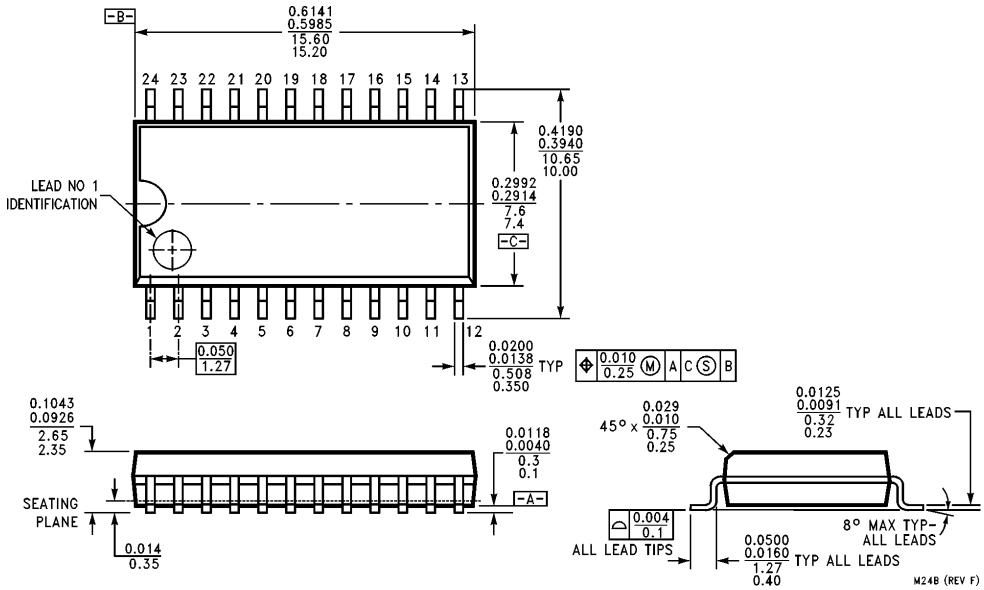
FIGURE 3. Simultaneous Switching Test Circuit

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

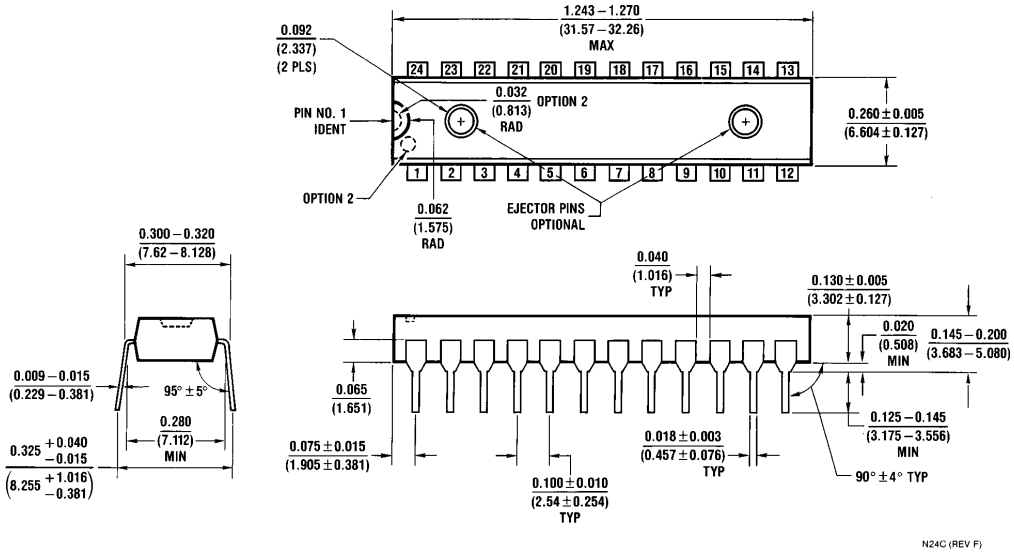


Physical Dimensions inches (millimeters)



24-Lead Small Outline Integrated Circuit (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)



24-Lead Slim (0.300″ Wide) Plastic Dual-In-Line Package (SP)
NS Package Number N24C

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