

# Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

# **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

D2932, MARCH 1987

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'F533 are transparent D-type latches. While the enable (C) is high, the  $\overline{\Omega}$  outputs will follow the complements of the D inputs. When the enable is taken low, the  $\overline{\Omega}$  outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'F533 is functionally equivalent to the 'F373 except for having inverted outputs.

A buffered output-control ( $\overline{OC}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

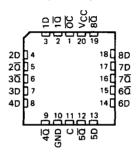
The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54F533 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74F533 is characterized for operation from 0°C to 70°C.

SN54F533 . . . J PACKAGE SN74F533 . . . DW OR N PACKAGE (TOP VIEW)

ठंट [[ा	U 20	□vcc
10 [ 2	19	<u> 0</u> 8
1D 🔲 3	18	8D
2D 🔲 4	. 17	] 7D
20 🗌 5	16	70
3₫ 🛮 6	15	] 6 <u>0</u>
3D 🔲 7	14	] 6D
4D 🛮 8	13	]5D
4₫ 🛮 9	12	5 <u>Q</u>
GND 🔯	0 11	]c

SN54F533 . . . FK PACKAGE



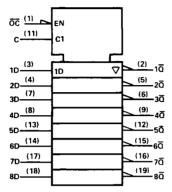
#### **FUNCTION TABLE (EACH LATCH)**

	INPUTS		OUTPUT
ōč	ENABLE C	D	ā
L	н	н	L .
L	н	L	н
L	L	×	σ̄ο
Н	x	х	Z

2

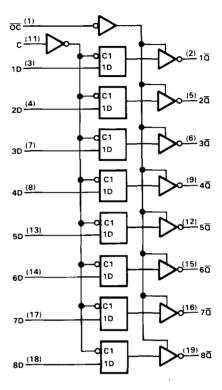
Data Sheets

## logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range

Supp	ly voltage, VCC	0.5 V to 7 V
Input	voltage †	1.2 V to 7 V
Input	current	-30 mA to 5 mA
Volta	ge applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Volta	ge applied to any output in the high state	0.5 to VCC
Curre	ent into any output in the low state: SN54F533	40 mA
	SN74F533	48 mA
Opera	ating free-air temperature range: SN54F533	-55°C to 125°C
	SN74F533	0°C to 70°C
Stora	de temperature rande	-65°C to 150°C

<sup>&</sup>lt;sup>†</sup>The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

	<del>-</del>		N54F53	3	s	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
ΊΚ	Input clamp current			- 18			- 18	mA
ЮН	High-level output current			- 3			~ 3	mA
loL	Low-level output current			20			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		9	13	S					
PARAMETER	TEST COND	MIN	TYP <sup>§</sup>	MAX	MIN	TYP§	MAX	UNIT	
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			- 1.2	V
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA	2.5	3.4		2.5	3.4		v
∨ <sub>ОН</sub> #	ν <sub>CC</sub> = 4.5 ν	IOH = -3 mA	2.4	3.3		2.4	3.3		v
Vai	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 mA		0.30	0.5				V
VOL		I <sub>OL</sub> = 24 mA					0.35	0.5	v
<sup>†</sup> OZH	$V_{CC} = 5.5 V$ ,	V <sub>O</sub> = 2.7 V			50			50	μΑ
<sup>I</sup> OZL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			- 50			- 50	μΑ
lj.	$V_{CC} = 5.5 V$ ,	V <sub>I</sub> = 7 V			0.1			0.1	mA
IH	$V_{CC} = 5.5 V$ ,	V <sub>I</sub> = 2.7 V			20			20	μΑ
կլ	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V			- 0.6			- 0.6	mA
los¶	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0	- 60		- 150	- 60		- 150	mA
Iccz	$V_{CC} = 5.5 V$ ,	See Note 1		41	61		41	61	mA

For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

<sup>§</sup> All typical values are at VCC = 5 V, TA = 25°C.

Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

<sup>#</sup> For the SN74F533 at  $V_{CC}=4.75$  V and  $I_{OH}=-1$  mA to -3 mA,  $V_{OH}$  min =2.7 V. NOTE 1:  $I_{CC}$  is measured with  $\overline{OC}$  at 4.5 V, all other inputs grounded.

# timing requirements

			V <sub>CC</sub> = 5 V, V <sub>CC</sub> = 4.5 V to 5.5 V, T <sub>A</sub> = 25 °C T <sub>A</sub> = MIN to MAX <sup>†</sup>					UNIT	
			'FE	33	SN54	IF533	SN74F533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	1
	Setup time before enable Ci	Data high	2		2		2		
tsu		or low							ns
	Hold time after enable C↓	Data high		_	3		3		
th	Hold time after enable C1	or low	3		3				ns
tw	Pulse duration	Enable C high	6		6		6		ns

# switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V.}$ $C_L = 50 \text{ pF,}$ $R1 \approx 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$ (F533		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = \text{MIN to MAX}^{\dagger}$ $SN54F533 \qquad SN74F533$ $MIN \qquad MAX \qquad MIN \qquad MAX$			UNIT			
tPLH		. *	3.2	6.5	9	3.2	12	3.2	10		
tPHL	D	D	Any 🖸	2.2	4.8	7	2.2	9	2.2	8	ns
tPLH		A	4.2	8.1	11	4.2	14	4.2	13		
tPHL	С	Any 🖸	2.2	5.2	. 7	2.2	9	2.2	8	ns	
tPZH	20	Any <b></b> ☐	1.2	7.3	10	1.2	12.5	1.2	11	ns	
tPZL_	OC	OC	Ally C	1.2	4.7	6.5	1.2	9	1.2	7.5	.,,
tPHZ_	20	Any Ō	1.2	4.3	6	1.2	8.5	1.2	7	ns	
<sup>t</sup> PLZ		Ally U	1.2	3.7	5.5	1.2	7.5	1.2	6.5	."	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions. NOTE 2: See General Information for load circuits and waveforms.