National Semiconductor

September 1990

MM74HCA240 Inverting Octal TRI-STATE® Buffer
MM74HCA241 Octal TRI-STATE® Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. Each has a fanout of 15 LS-TTL equivalent inputs.

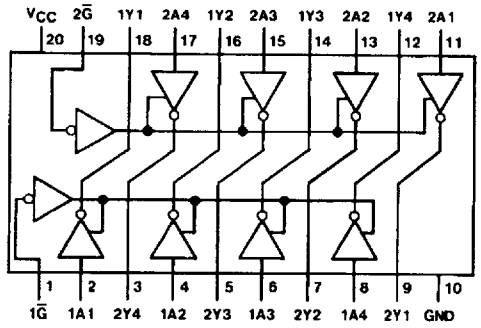
The MM74HCA240 is an inverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls 4 buffers. MM74HCA241 is a non-inverting buffer that has one active low enable and one active high enable, each again controlling 4 buffers. Neither device has Schmitt trigger inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 40 μA
- Output current: 6 mA
- Low output noise generation
- QOS specification V_{OLV}, V_{OLP}
- Identical pinout to HC
- Speed upgrade to HC

Connection Diagrams Dual-In-Line Packages



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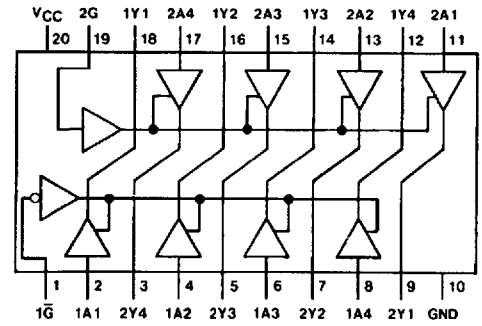
Order Number MM74HCA240



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Truth Table

HCA240

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

HCA241

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	H	Z	H	H	H
H	H	Z	H	H	Z

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCA	−40	+85	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HCA T_A = −40 to 85°C		Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			3.0V		2.1	2.1	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.5	0.5	V
			3.0V		0.9	0.9	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			3.0V	3.0	2.9	2.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	3.0V	2.78	2.68	2.63	V
		$\|I_{OUT}\| \leq 7.8$ mA	4.5V	4.28	4.18	4.13	V
			6.0V	5.78	5.68	5.63	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	V
			3.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	3.0V	0.2	0.26	0.33	V
		$\|I_{OUT}\| \leq 7.8$ mA	4.5V	0.2	0.26	0.33	V
			6.0V	0.2	0.26	0.33	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}, G = V_{IL}	6.0V		±0.5	±5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	μA
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	*Figures 1, 2* (Note 5)	5.5		+0.550		V
V_{OLV}	Quiet Output Maximum Dynamic V_{OL}	*Figures 1, 2* (Note 5)	5.5		−0.750		V

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HCA at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Note 5: n = number of device outputs, n − 1 outputs switching, each driven 0V to 5.5V, one output @ ground

AC Electrical Characteristics MM74HCA240 $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	11	17	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ $C_L=45$ pF	14	24	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	$R_L=1$ kΩ $C_L=5$ pF	14	24	ns

AC Electrical Characteristics MM74HCA240

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HCA $T_A=-40$ to 85°C		Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	36	90	115	ns
		$C_L=150$ pF	2.0V	51	130	165	ns
		$C_L=50$ pF	3.3V	18	27	35	ns
		$C_L=150$ pF	3.3V	26	39	50	ns
		$C_L=50$ pF	4.5V	12	18	23	ns
		$C_L=150$ pF	4.5V	17	26	33	ns
		$C_L=50$ pF	6.0V	11	15	20	ns
		$C_L=150$ pF	6.0V	16	22	28	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ					
		$C_L=50$ pF	2.0V	45	125	155	ns
		$C_L=150$ pF	2.0V	60	165	205	ns
		$C_L=50$ pF	3.3V	23	38	47	ns
		$C_L=150$ pF	3.3V	30	50	62	ns
		$C_L=50$ pF	4.5V	15	25	31	ns
		$C_L=150$ pF	4.5V	20	33	41	ns
		$C_L=50$ pF	6.0V	13	21	26	ns
		$C_L=150$ pF	6.0V	17	28	35	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	45	125	155	ns
			3.3V	23	38	47	ns
			4.5V	15	25	31	ns
			6.0V	13	21	26	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	ns
			3.3V		60	75	ns
			4.5V		12	15	ns
			6.0V		10	13	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer) $\overline{G}=V_{IH}$		12			pF
		$\overline{G}=V_{IL}$		50			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF
C_{OUT}	Maximum Output Capacitance			10			pF

AC Electrical Characteristics MM74HCA241 $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF		14	17	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ	$1\overline{G}$	14	24	ns
		$C_L=45$ pF	$2\overline{G}$	14	24	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Input	$R_L=1$ kΩ	$1\overline{G}$	14	24	ns
		$C_L=5$ pF	$2\overline{G}$	14	24	ns

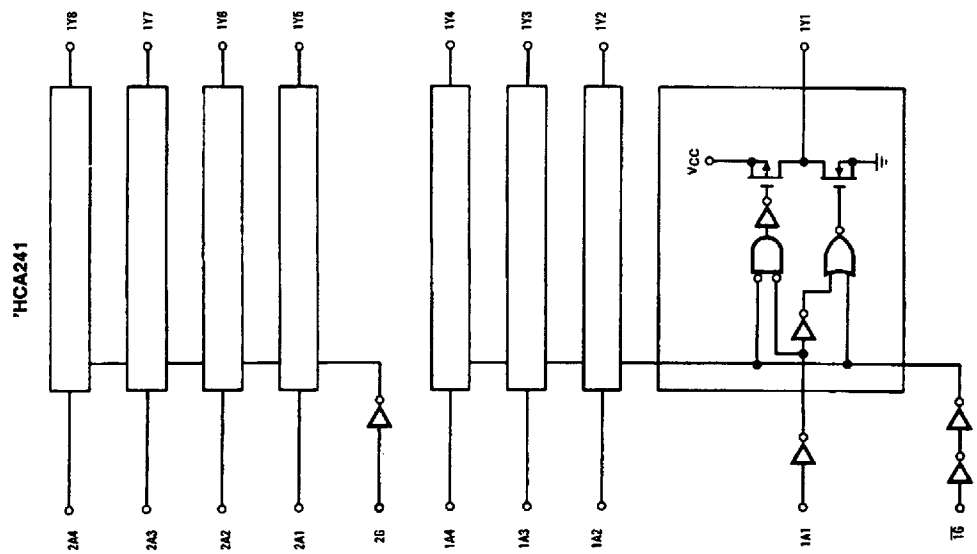
AC Electrical Characteristics MM74HCA241

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HCA $T_A=-40$ to 85°C		Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	42	90	115	ns
		$C_L=150$ pF	2.0V	51	130	165	ns
		$C_L=50$ pF	3.3V	21	27	35	ns
		$C_L=150$ pF	3.3V	26	39	50	ns
		$C_L=50$ pF	4.5V	14	18	23	ns
		$C_L=150$ pF	4.5V	17	26	33	ns
		$C_L=50$ pF	6.0V	10	15	20	ns
		$C_L=150$ pF	6.0V	14	22	28	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ					
		$C_L=50$ pF	2.0V	45	125	155	ns
		$C_L=150$ pF	2.0V	103	165	205	ns
		$C_L=50$ pF	3.3V	23	38	47	ns
		$C_L=150$ pF	3.3V	32	50	62	ns
		$C_L=50$ pF	4.5V	15	25	31	ns
		$C_L=150$ pF	4.5V	21	33	41	ns
		$C_L=50$ pF	6.0V	13	21	26	ns
		$C_L=150$ pF	6.0V	17	28	35	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	45	125	155	ns
		$C_L=50$ pF	3.3V	23	38	47	ns
			4.5V	15	25	31	ns
			6.0V	13	21	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	ns
			3.3V		60	75	ns
			4.5V		12	15	ns
			6.0V		10	13	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)					
		$G=V_{IL}$, $\overline{G}=V_{IH}$		12			pF
		$G=V_{IH}$, $\overline{G}=V_{IL}$		50			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF
C_{OUT}	Maximum Output Capacitance			10			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



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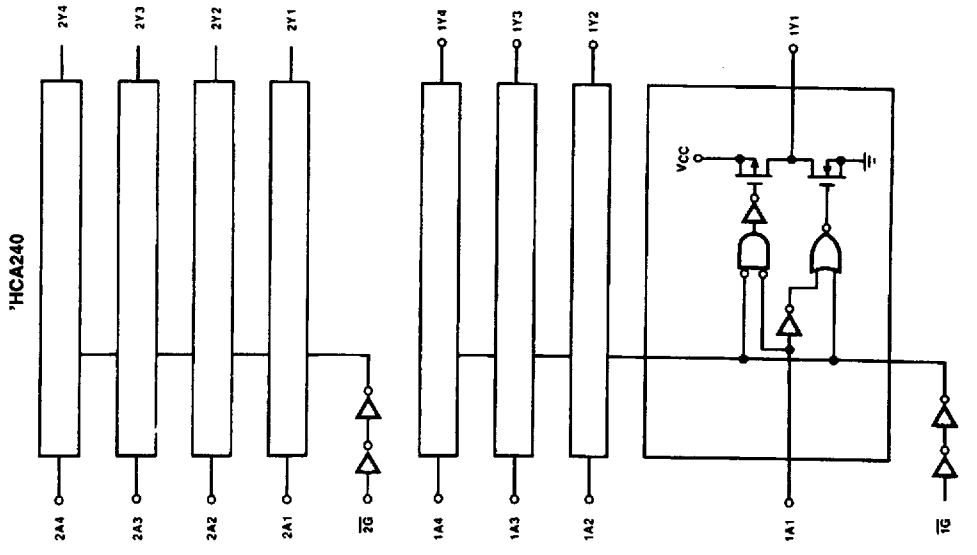

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HCA Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of HCA.

Equipment:

Word Generator
Printed Circuit Board Test Fixture
Dual Trace Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 5.5V HIGH for HCA devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

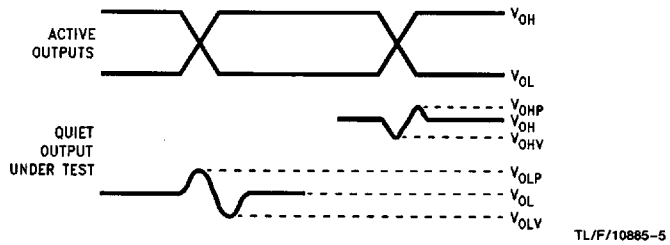


FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A. V_{OLV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

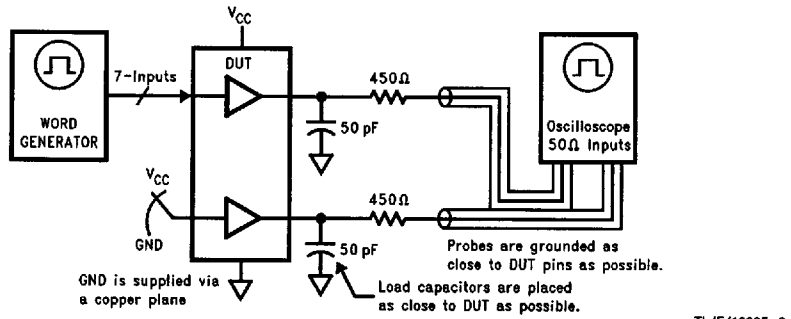
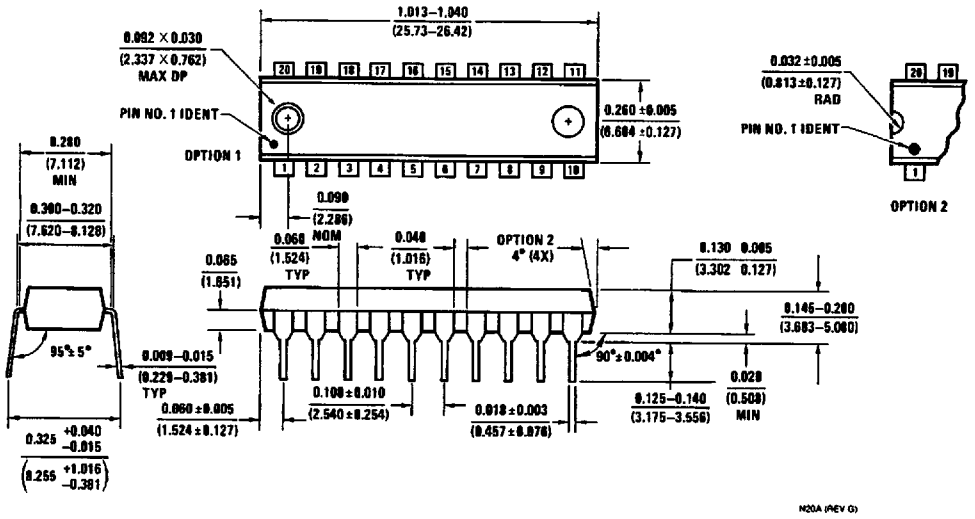


FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters)



Order Number MM74HCA240N or MM74HCA241N
NS Package Number N20A

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