

SN54BCT2828B, SN74BCT2828B 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING OUTPUTS

D3635, SEPTEMBER 1990

- BICMOS Design Substantially Reduces I_{CC}
- Output Ports Have Equivalent 25- Ω Resistors, So No External Resistors Are Required
- Specifically Designed to Drive MOS DRAMs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Data Flow-Thru Pinout (All Inputs on Opposite Side From Outputs)
- Power-Up High-Impedance State
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

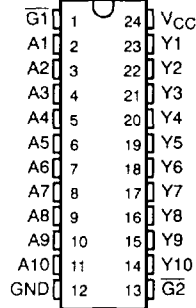
The 3-state control gate is a 2-input AND gate with active-low inputs so if either $\overline{G1}$ or $\overline{G2}$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

The SN54BCT2828B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT2828B is characterized for operation from 0°C to 70°C .

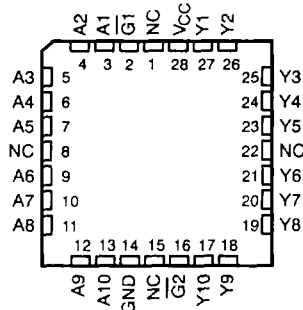
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G1}$	$\overline{G2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

SN54BCT2828B . . . JT PACKAGE
SN74BCT2828B . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT2828B . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCT PREVIEW

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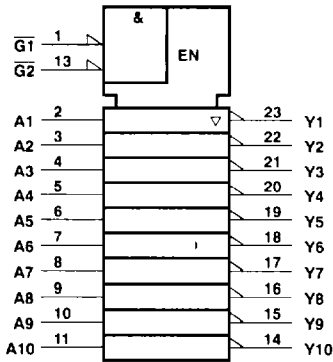


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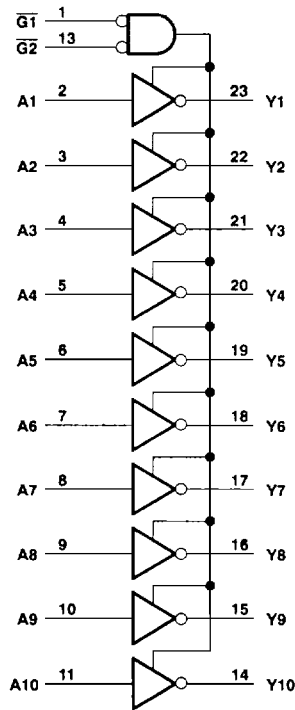
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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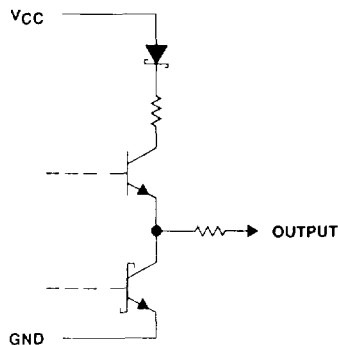
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SN54BCT2828B, SN74BCT2828B
10-BIT BUS/MOS MEMORY DRIVERS
WITH 3-STATE INVERTING OUTPUTS

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schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	- 0.5 V to 7 V
Input voltage range (see Note 1)	- 0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	- 0.5 V to 5.5 V
Voltage applied to any output in the high state	- 0.5 V to V_{CC}
Input clamp current	- 30 mA
Current into any output in the low state	24 mA
Operating free-air temperature range: SN54BCT2828B	- 55°C to 125°C
SN74BCT2828B	0°C to 70°C
Storage temperature range	- 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage ratings may be exceeded if the input clamp current ratings is observed.

recommended operating conditions

		SN54BCT2828B			SN74BCT2828B			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage	0.8			0.8			V	
I_{IK}	Input clamp current	- 18			- 18			mA	
I_{OH}	High-level output current	- 1			- 1			mA	
I_{OL}	Low-level output current	12			12			mA	
T_A	Operating free-air temperature	- 55			0			70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT2828B			SN74BCT2828B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$I_{OH} = -1 \text{ mA}$	V_{CC}^{-2}			V_{CC}^{-2}			V
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 1 \text{ mA}$		0.15	0.5		0.15	0.5	V
		$I_{OL} = 12 \text{ mA}$		0.35	0.8		0.35	0.8	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$,	$V_O = 0.5 \text{ V}$			-20			-20	μA
$I_{OL(sink)}$	$V_{CC} = 4.5 \text{ V}$,	$V_O = 2 \text{ V}$	50			50			mA
I_I	$V_{CC} = 5.5 \text{ V}$,	$V_O = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.5 \text{ V}$			-0.2			-0.2	mA
$I_{O\ddagger}$	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.25 \text{ V}$	-30		-112	-30		-112	mA
I_{CCL}	$V_{CC} = 5.5 \text{ V}$,	Outputs open		28			28		mA
I_{CCZ}	$V_{CC} = 5.5 \text{ V}$,	Outputs open		3.5			3.5		mA
C_i	$V_{CC} = 5 \text{ V}$,	$V_I = 2.5 \text{ V or } 0.5 \text{ V}$		5			5		pF
C_o				8			8		pF

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS} .

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